Électronique

Étude de la PLL CD4046B

Introduction

La PLL CD4046B est une boucle à verrouillage de phase de type numérique : les signaux d'entrée doivent être carrés. Dans l'étude qui suit il est possible de choisir entre deux comparateurs : le OU EXCLUSIF et le comparateur 2 à logique séquentielle (dont vous trouverez le fonctionnement détaillé dans la documentation technique du HEF 4046B). Le VCO possède une grande gamme de variation de fréquence qui peut être réglée en pratique à l'aide des résistances R_1 et R_2 et de la capacité C_1 . Le circuit est alimenté sous 10 V : $V_{dd} = 10$ V et $V_{ss} = 0$ V.

L'étude suivante va permettre de vérifier quelques propriétés de la PLL CD4046B à l'aide de LTspice et de modèles déjà réalisés. Les fichiers nécessaires se trouvent dans l'archive "CD4046B.zip". Il est nécessaire de conserver l'ensemble des fichiers dans le même dossier.

Les paramètres de simulation sont déjà réglés et il suffit de lancer la simulation après avoir éventuellement ajusté les valeurs de fréquence ou les valeurs des composants.

1 Caractérisation du VCO

1. À partir de la notice technique de la PLL HEF 4046B (similaire à la PLL CD4046B) fournie à la fin de ce document, déterminer pour une capacité $C_1 =$ 1 nF, et des résistances $R_1 = 10$ kΩ et R_2 infinie, la plage de fonctionnement du VCO.

2. Introduire les valeurs obtenues de $f_{\min}$ et $f_{\max}$ dans les caractéristiques du modèle LTSpice de la PLL CD4046B (fichier de simulation "CD4046B_VCO.asc"), et vérifier le bon fonctionnement de la simulation du VCO en relevant sa caractéristique. On prendra pour la tension d'entrée V1 des valeurs de 0 à 10 V par pas de 1 V. On mesurera la fréquence du signal fvco en sortie du VCO en utilisant la fonction FFT de LTSpice.

2 Mesure des plages de capture et de verrouillage

La mesure des plages de capture et de verrouillage va s'effectuer en utilisant une simulation temporelle durant laquelle la fréquence d'entrée de la PLL va varier linéairement. Chaque point correspond ainsi à une fréquence d'entrée. Le fichier de simulation contient un montage permettant de générer un signal de fréquence déterminée, et la PLL à proprement parler. Le changement de comparateur de phase s'opère en renommant l'entrée du filtre.

3. Dans le fichier de simulation "CD4046B_sweep_croissant.asc" réaliser la simulation pour les deux comparateurs et pour les deux valeurs de la capacité $C_2 = 10$ nF et 100 nF (la simulation est assez longue). Afficher dans la fenêtre graphique V(freqcontrol) et V(vco_in). Exporter les données au format texte (clic droit sur la figure puis File → Export data as text).

4. Refaire les mêmes simulations pour un sweep décroissant en utilisant le fichier de simulation "CD4046B_sweep_decroissant.asc". Exporter à nouveau les données au format texte.

5. Importer les données enregistrées au format texte sous Excel (ou tout autre logiciel permettant de traiter de données). À l'aide de la caractéristique du VCO obtenue dans la partie 1, tracer pour chacun des 4 cas traités la courbe d'hystérésis f_s (en sortie du VCO) en fonction de f_e (fréquence du signal d'entrée). En déduire les plages de capture et de verrouillage de la PLL pour chacun des cas.

3 Réponse de la PLL à un échelon

1. Dans le fichier de simulation "CD4046B_echelon.asc" réaliser la simulation pour les deux comparateurs et pour les deux valeurs de la capacité $C_2 = 10$ nF et 100 nF. Afficher dans la fenêtre graphique V(freqcontrol) et V(vco_in).

2. Mesurer sur V(vco_in), pour chacun des cas traités, le temps nécessaire pour atteindre 90% de la valeur de V(freqcontrol).

3. Comparer les résultats obtenus à la question précédente aux temps caractéristiques des filtres utilisés.

INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4046B
MSI
Phase-locked loop

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Phase-locked loop

HEF4046B MSI

DESCRIPTION

The HEF4046B is a phase-locked loop circuit that consists of a linear voltage controlled oscillator (VCO) and two different phase comparators with a common signal input amplifier and a common comparator input. A 7 V regulator (zener) diode is provided for supply voltage regulation if necessary. For functional description see further on in this data.

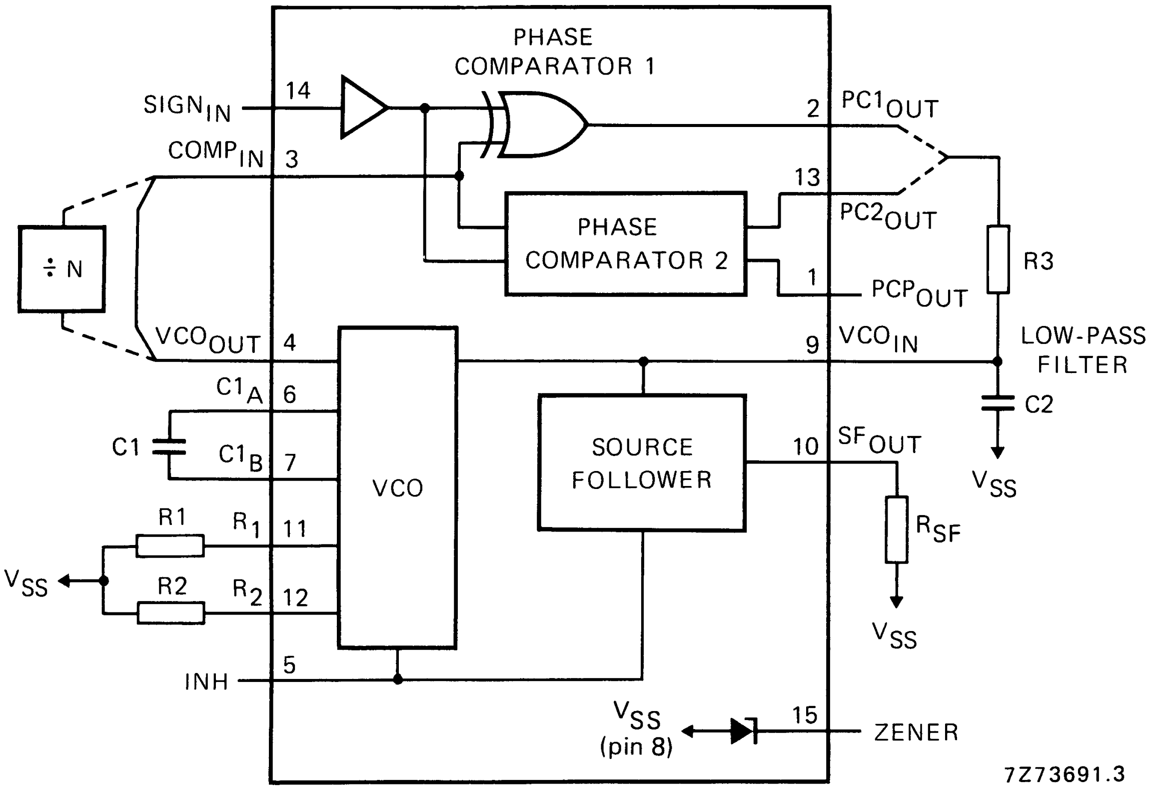


Fig.1 Functional diagram.

HEF4046BP(N):	16-lead DIL; plastic (SOT38-1)
HEF4046BD(F):	16-lead DIL; ceramic (cerdip) (SOT74)
HEF4046BT(D):	16-lead SO; plastic (SOT109-1)

( ): Package Designator North America

FAMILY DATA

See Family Specifications

I_{DD} LIMITS category MSI

See further on in this data.

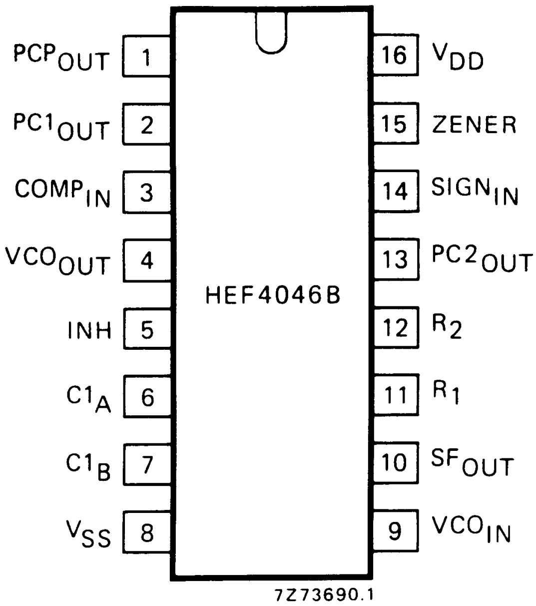


Fig.2 Pinning diagram.

PINNING

1. Phase comparator pulse output
2. Phase comparator 1 output
3. Comparator input
4. VCO output
5. Inhibit input
6. Capacitor C1 connection A
7. Capacitor C1 connection B
8. V_{SS}
9. VCO input
10. Source-follower output
11. Resistor R1 connection
12. Resistor R2 connection
13. Phase comparator 2 output
14. Signal input
15. Zener diode input for regulated supply.

FUNCTIONAL DESCRIPTION

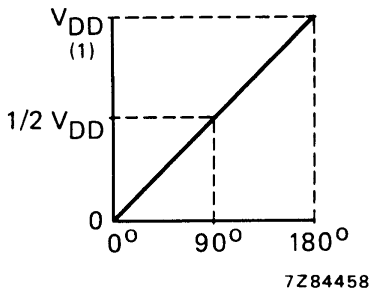
VCO part

The VCO requires one external capacitor (C1) and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency off-set if required. The high input impedance of the VCO simplifies the design of low-pass filters; it permits the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at pin 10. If this pin (SF_{OUT}) is used, a load resistor (R_{SF}) should be connected from this pin to V_{SS}; if unused, this pin should be left open. The VCO output (pin 4) can either be connected directly to the comparator input (pin 3) or via a frequency divider. A LOW level at the inhibit input (pin 5) enables the VCO and the source follower, while a HIGH level turns off both to minimize stand-by power consumption.

Phase comparators

The phase-comparator signal input (pin 14) can be direct-coupled, provided the signal swing is between the standard HE4000B family input logic levels. The signal must be capacitively coupled to the self-biasing amplifier at the signal input in case of smaller swings. Phase comparator 1 is an EXCLUSIVE-OR network. The signal and comparator input frequencies must have a 50% duty factor to obtain the maximum lock range. The average output voltage of the phase comparator is equal to ½ V_{DD} when there is no signal or noise at the signal input. The average voltage to the VCO input is supplied by the low-pass filter connected to the output of phase comparator 1. This also causes the VCO to oscillate at the centre frequency (f_o). The frequency capture range (2 f_c) is defined as the frequency range of input signals on which the PLL will lock if it was initially out of lock. The frequency lock range (2 f_L) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With phase comparator 1, the range of frequencies over which the PLL can acquire lock (capture range) depends on the low-pass filter characteristics and this range can be made as large as the lock range. Phase comparator 1 enables the PLL system to remain in lock in spite of high amounts of noise in the input signal. A typical behaviour of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO centre frequency. Another typical behaviour is, that the phase angle between the signal and comparator input varies between 0° and 180° and is 90° at the centre frequency. Figure 3 shows the typical phase-to-output response characteristic.



(1) Average output voltage.

Fig.3 Signal-to-comparator inputs phase difference for comparator 1.

Figure 4 shows the typical waveforms for a PLL employing phase comparator 1 in locked condition of f_o.

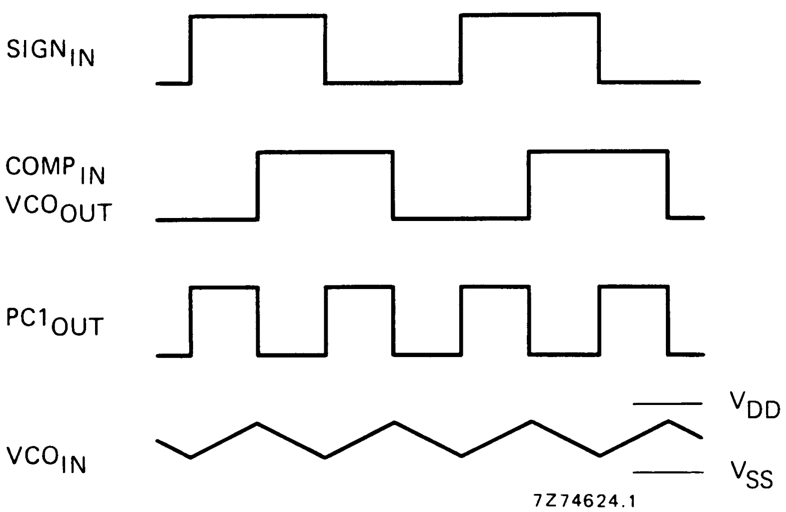


Fig.4 Typical waveforms for phase-locked loop employing phase comparator 1 in locked condition of f_o.

Phase comparator 2 is an edge-controlled digital memory network. It consists of four flip-flops, control gating and a 3-state output circuit comprising p and n-type drivers having a common output node. When the p-type or n-type drivers are ON, they pull the output up to V_{DD} or down to V_{SS} respectively. This type of phase comparator only acts on the positive-going edges of the signals at $SIGN_{IN}$ and $COMP_{IN}$. Therefore, the duty factors of these signals are not of importance.

If the signal input frequency is higher than the comparator input frequency, the p-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF (3-state) the remainder of the time. If the signal input frequency is lower than the comparator input frequency, the n-type output driver is maintained ON most of the time, and both the n and p-type drivers are OFF the remainder of the time. If the signal input and comparator input frequencies are equal, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the comparator input lags the signal input in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the voltage at the capacitor of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point, both p and n-type drivers remain OFF and thus the phase comparator output becomes an open circuit and keeps the voltage at the capacitor of the low-pass filter constant.

Moreover, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level which can be used for indicating a locked condition. Thus, for phase comparator 2 no phase difference exists between the signal and comparator inputs over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both p and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator 2 . Figure 5 shows typical waveforms for a PLL employing this type of phase comparator in locked condition.

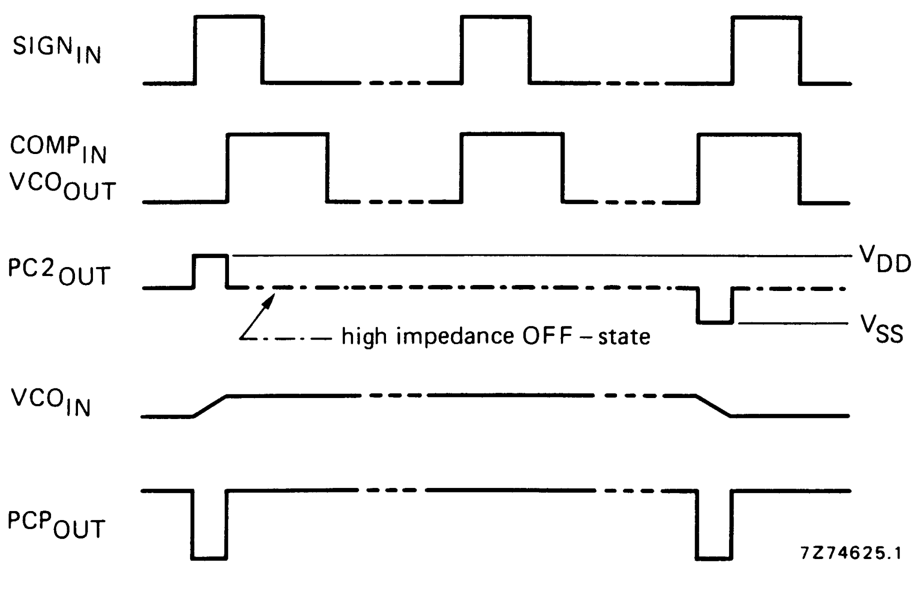
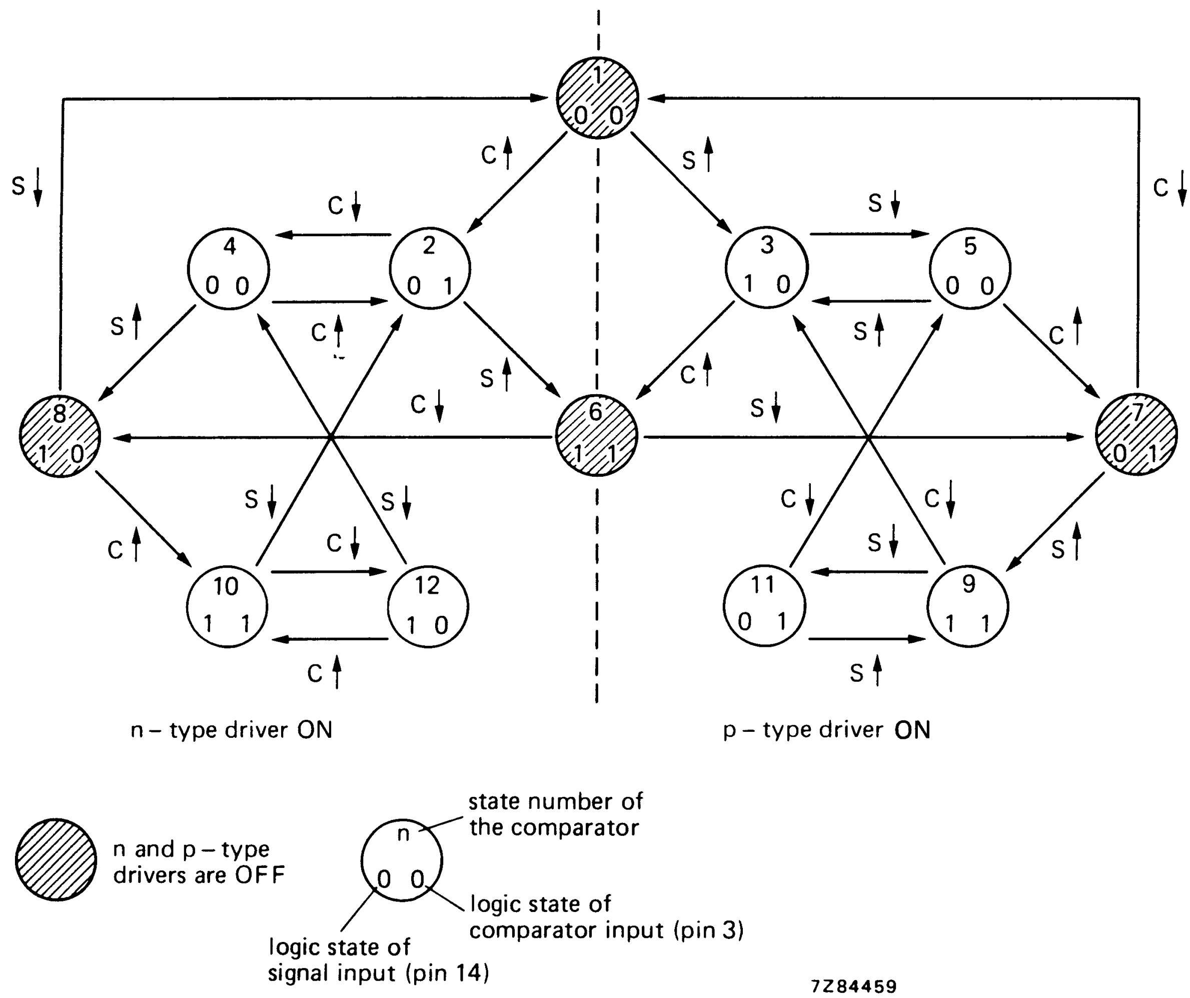


Fig.5 Typical waveforms for phase-locked loop employing phase comparator 2 in locked condition.

Figure 6 shows the state diagram for phase comparator 2. Each circle represents a state of the comparator. The number at the top, inside each circle, represents the state of the comparator, while the logic state of the signal and comparator inputs are represented by a ‘0’ for a logic LOW or a ‘1’ for a logic HIGH, and they are shown in the left and right bottom of each circle.

The transitions from one to another result from either a logic change at the signal input (S) or the comparator input (C). A positive-going and a negative-going transition are shown by an arrow pointing up or down respectively.

The state diagram assumes, that only one transition on either the signal input or comparator input occurs at any instant. States 3, 5, 9 and 11 represent the condition at the output when the p-type driver is ON, while states 2, 4, 10 and 12 determine the condition when the n-type driver is ON. States 1, 6, 7 and 8 represent the condition when the output is in its high impedance OFF state; i.e. both p and n-type drivers are OFF, and the PCP_{OUT} output is HIGH. The condition at output PCP_{OUT} for all other states is LOW.



S ↑: 0 to 1 transition at the signal input.
C ↓ : 1 to 0 transition at the comparator input.

Fig.6 State diagram for comparator 2.

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	SYMBOL	T_{amb} (°C) −40 TYP.	−40 MAX.	+ 25 TYP.	+ 25 MAX.	+ 85 TYP.	+ 85 MAX.	
Supply current	5		–	–	20	–	–	–	μA
(note 1)	10	I_D	–	–	300	–	–	–	μA
	15		–	–	750	–	–	–	μA
Quiescent device	5		–	20	–	20	–	150	μA
current (note 2)	10	I_{DD}	–	40	–	40	–	300	μA
	15		–	80	–	80	–	600	μA

Notes

1. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 open.
2. Pin 15 open; pin 5 at V_{DD}; pins 3 and 9 at V_{SS}; pin 14 at V_{DD}; input current pin 14 not included.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		
Phase comparators							
Operating supply voltage		V_{DD}	3		15	V	
Input resistance	5			750		kΩ	at self-bias operating point
at $SIGN_{IN}$	10	R_{IN}		220		kΩ	
	15			140		kΩ	
A.C. coupled input	5			150		mV	peak-to-peak values; R1 = 10 kΩ; R2 = ∞; C1 = 100 pF; independent of the lock range
sensitivity	10	V_{IN}		150		mV	
at $SIGN_{IN}$	15			200		mV	
D.C. coupled input sensitivity							full temperature range
at $SIGN_{IN}$; $COMP_{IN}$	5				1,5	V	
LOW level	10	V_{IL}			3,0	V	
	15				4,0	V	
	5		3,5			V	
HIGH level	10	V_{IH}	7,0			V	
	15		11,0			V	
Input current	5			7		μA	$SIGN_{IN}$ at V_{DD}
at $SIGN_{IN}$	10	$+ I_{IN}$		30		μA	
	15			70		μA	
	5			3		μA	$SIGN_{IN}$ at V_{SS}
	10	$-I_{IN}$		18		μA	
	15			45		μA	

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.			
VCO								
Operating supply voltage		V_{DD}	3		15	V	as fixed oscillator only	
			5		15	V	phase-locked loop operation	
Power dissipation	5			150		µW	f_o = 10 kHz; R1 = 1 MΩ;	
	10	P		2500		µW	R2 = ∞; VCO_{IN} at ½ V_{DD};	
	15			9000		µW	see also Figs 10 and 11	
Maximum operating frequency	5		0,5	1,0		MHz	VCO_{IN} at V_{DD};	
	10	f_{max}	1,0	2,0		MHz	R1 = 10 kΩ; R2 = ∞;	
	15		1,3	2,7		MHz	C1 = 50 pF	
Temperature/ frequency stability	5			0,22—0,30		%/°C	no frequency offset	
	10			0,04—0,05		%/°C	(f_{min} = 0);	
	15			0,01—0,05		%/°C	see also note 1	
	5			0—0,22		%/°C	with frequency offset	
	10			0—0,04		%/°C	(f_{min} > 0);	
	15			0—0,01		%/°C	see also note 1	
Linearity	5			0,50		%	R1 > 10 kΩ	see Fig.13
	10			0,25		%	R1 > 400 kΩ	and Figs 14
	15			0,25		%	R1 = 1 MΩ	15 and 16
Duty factor at VCO_{OUT}	5			50		%		
	10	δ		50		%		
	15			50		%		
Input resistance at VCO_{IN}	5			10^6		MΩ		
	10	R_{IN}		10^6		MΩ		
	15			10^6		MΩ		
Source follower								
Offset voltage VCO_{IN} minus SF_{OUT}	5			1,7		V	R_{SF} = 10 kΩ;	
	10			2,0		V	VCO_{IN} at ½ V_{DD}	
	15			2,1		V		
	5			1,5		V	R_{SF} = 50 kΩ;	
	10			1,7		V	VCO_{IN} at ½ V_{DD}	
	15			1,8		V		
Linearity	5			0,3		%	R_{SF} > 50 kΩ;	
	10			1,0		%	see Fig.13	
	15			1,3		%		
Zener diode								
Zener voltage		V_Z		7,3		V	I_Z = 50 µA	
Dynamic resistance		R_Z		25		Ω	I_Z = 1 mA	

Notes

1. Over the recommended component range.

DESIGN INFORMATION

CHARACTERISTIC	USING PHASE COMPARATOR 1	USING PHASE COMPARATOR 2
No signal on $SIGN_{IN}$	VCO in PLL system adjusts to centre frequency (f_o)	VCO in PLL system adjusts to min. frequency (f_{min})
Phase angle between $SIGN_{IN}$ and $COMP_{IN}$	90° at centre frequency (f_o), approaching 0° and 180° at ends of lock range (2 f_L)	always 0° in lock (positive-going edges)
Locks on harmonics of centre frequency	yes	no
Signal input noise rejection	high	low
Lock frequency range (2 f_L)	the frequency range of the input signal on which the loop will stay locked if it was initially in lock; 2 f_L = full VCO frequency range = $f_{max} - f_{min}$	
Capture frequency range (2 f_C)	the frequency range of the input signal on which the loop will lock if it was initially out of lock	
	depends on low-pass filter characteristics; $f_C < f_L$	$f_C = f_L$
Centre frequency (f_o)	the frequency of the VCO when VCO_{IN} at ½V_{DD}	

VCO component selection

Recommended range for R1 and R2: 10 kΩ to 1 MΩ; for C1: 50 pF to any practical value.

1. VCO without frequency offset (R2 = ∞).
   a) Given f_o: use f_o with Fig.7 to determine R1 and C1.
   b) Given f_{max}: calculate f_o from $f_o = \frac{1}{2} f_{max}$; use f_o with Fig.7 to determine R1 and C1.
2. VCO with frequency offset.
   a) Given f_o and f_L : calculate f_{min} from the equation $f_{min} = f_o - f_L$; use f_{min} with Fig.8 to determine R2 and C1; calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$; use $\frac{f_{max}}{f_{min}}$ with Fig. 9 to determine the ratio R2/R1 to obtain R1.
   b) Given f_{min} and f_{max}: use f_{min} with Fig.8 to determine R2 and C1; calculate

   $\frac{f_{max}}{f_{min}}$; use $\frac{f_{max}}{f_{min}}$

   with Fig.9 to determine R2/R1 to obtain R1.

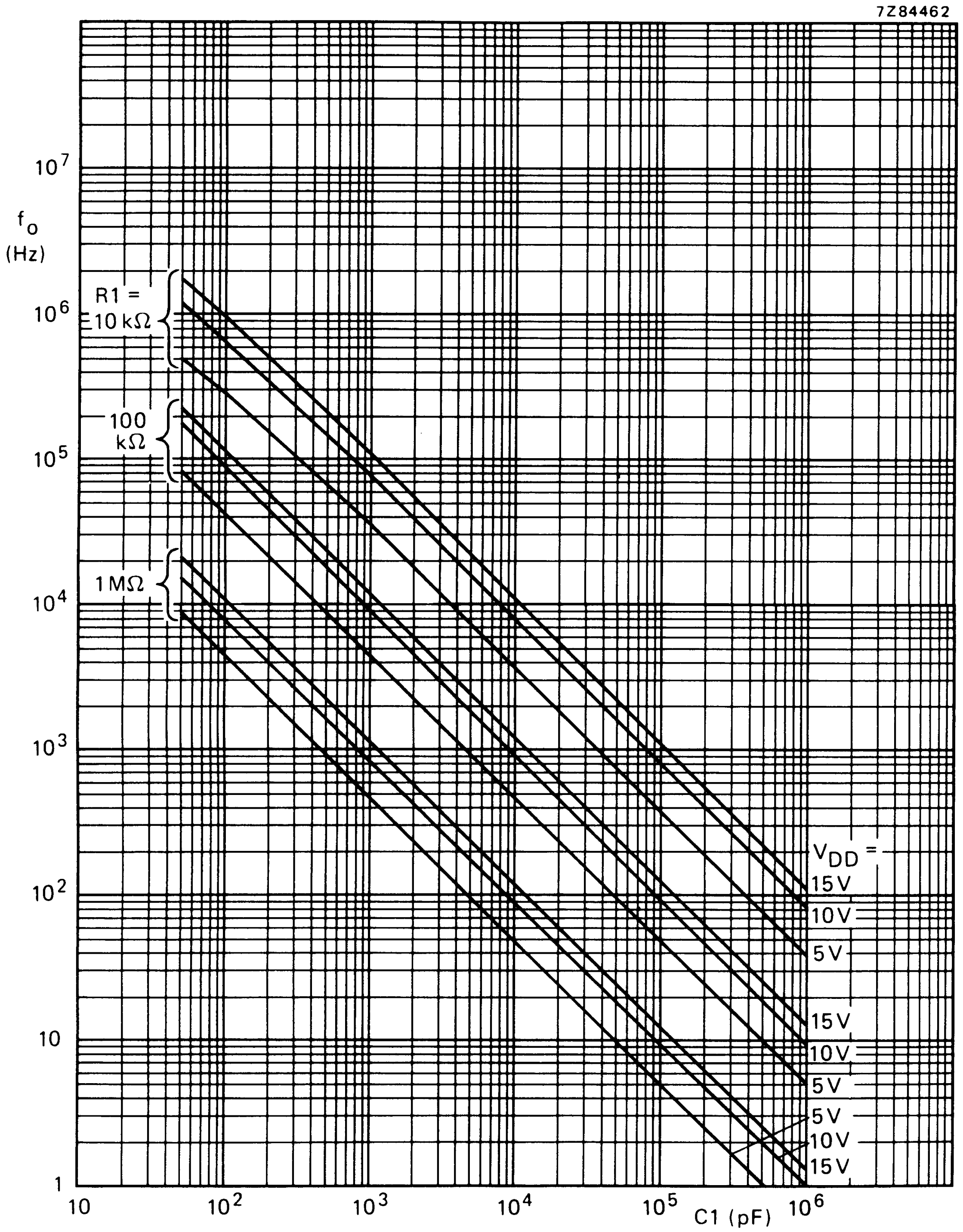


Fig.7 Typical centre frequency as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at ½ V_{DD}; INH at V_{SS}; R_2 = ∞.

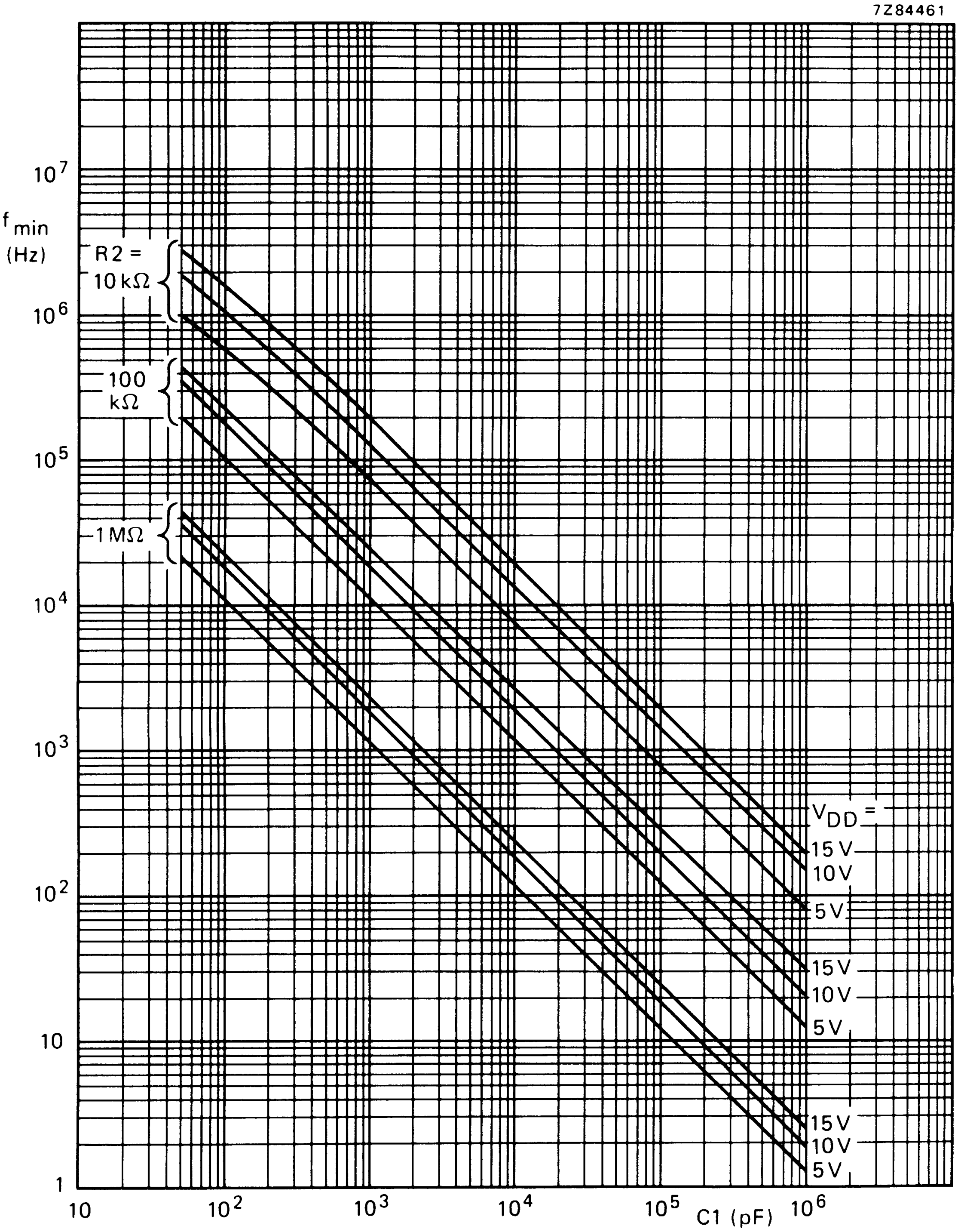


Fig.8 Typical frequency offset as a function of capacitor C1; T_{amb} = 25 °C; VCO_{IN} at V_{SS}; INH at $V_{SS;}$ R1 = ∞.

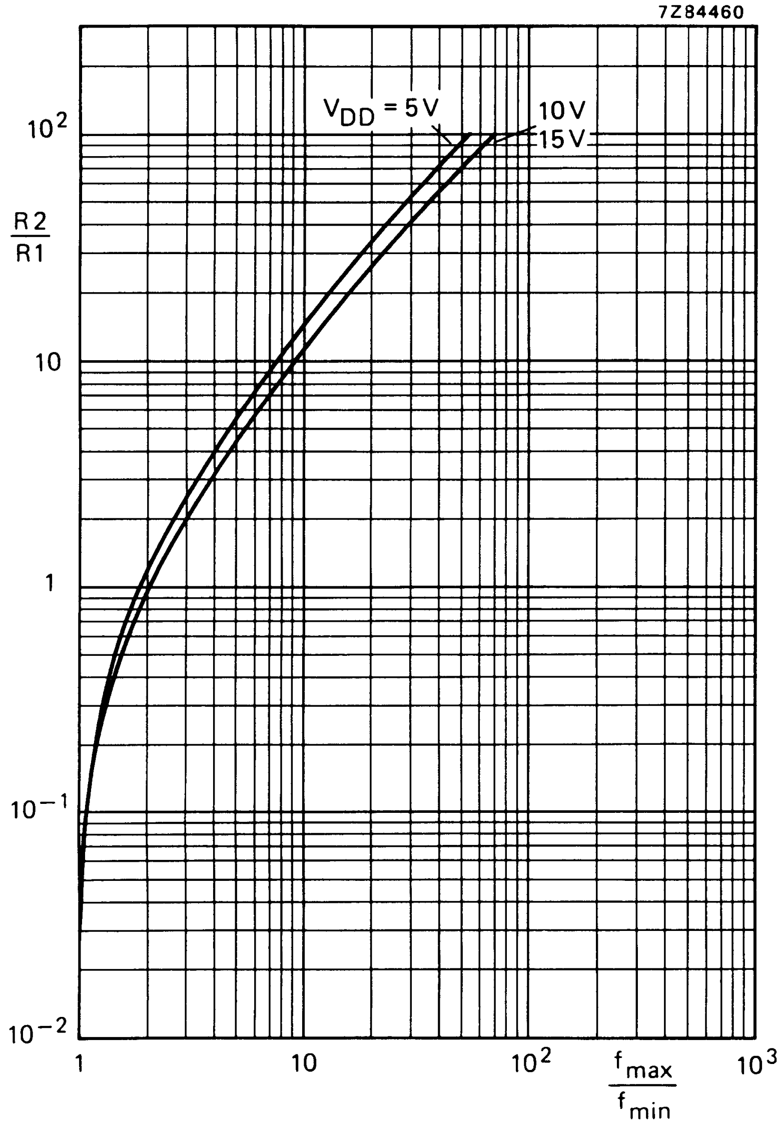


Fig.9 Typical ratio of R2/R1 as a function of the ratio f_{max}/f_{min}.

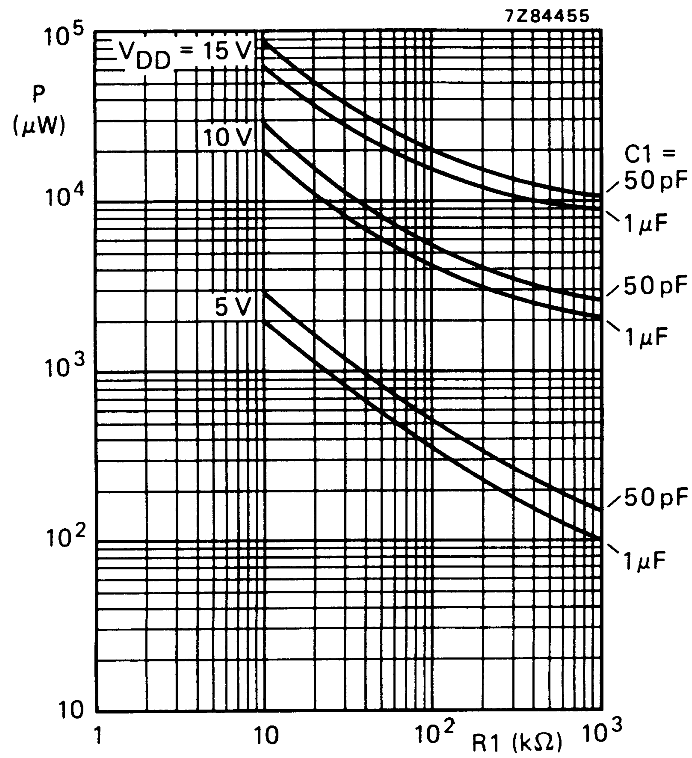


Fig.10 Power dissipation as a function of R1; R2 = ∞; VCO_{IN} at ½ V_{DD}; C_L = 50 pF.

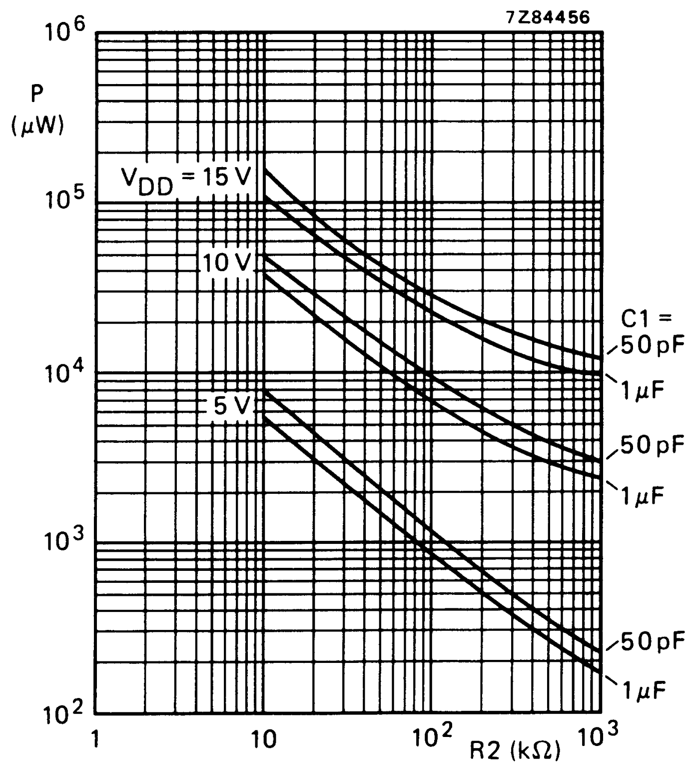


Fig.11 Power dissipation as a function of R2; R1 = ∞; VCO_{IN} at V_{SS} (0 V); C_L = 50 pF.

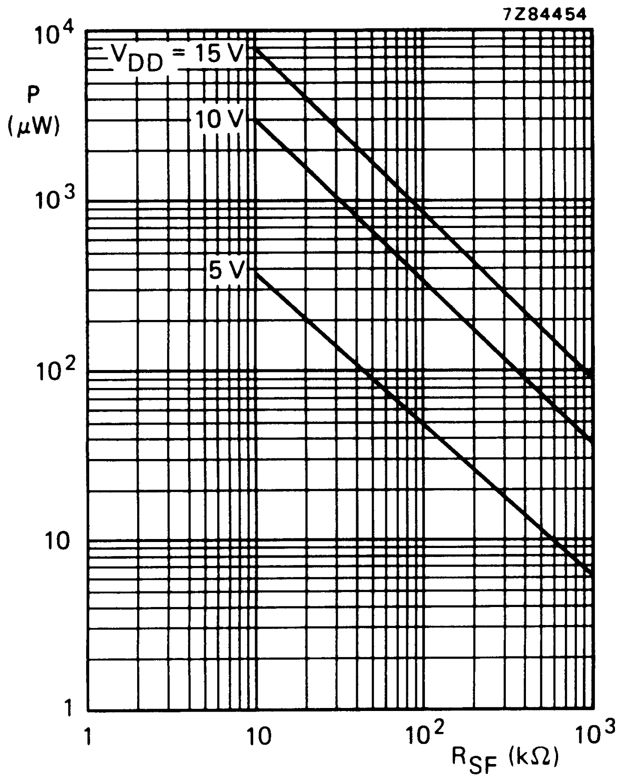


Fig.12 Power dissipation of source follower as a function of R_{SF}; VCO_{IN} at ½ V_{DD}; R1 = ∞ ; R2 = ∞ .

For VCO linearity:

$$f_o' = \frac{f_1 + f_2}{2}$$

$$\text{lin.} = \frac{f_o' - f_o}{f_o'} \times 100\%$$

Figure 13 and the above formula also apply to source follower linearity: substitute $V_{SF\ OUT}$ for f.

ΔV = 0,3 V at V_{DD} = 5 V
ΔV = 2,5 V at V_{DD} = 10 V
ΔV = 5 V at V_{DD} = 15 V

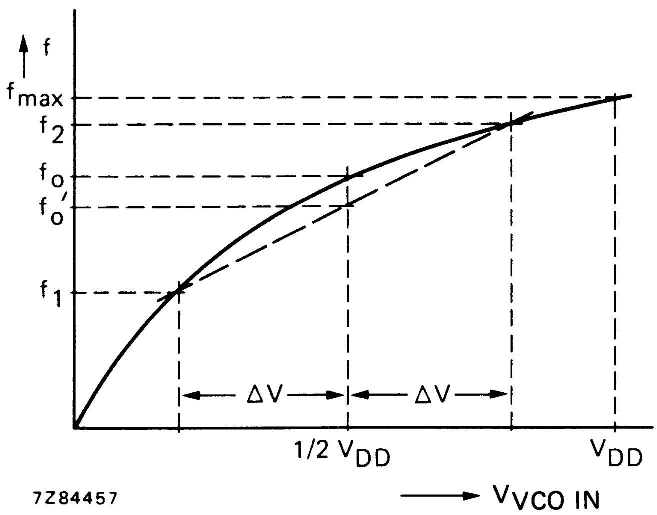


Fig.13 Definition of linearity (see AC characteristics).

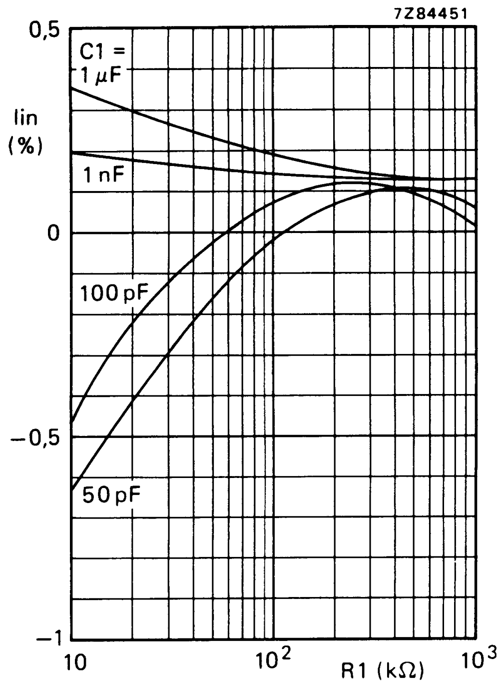


Fig.14 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 5 V.

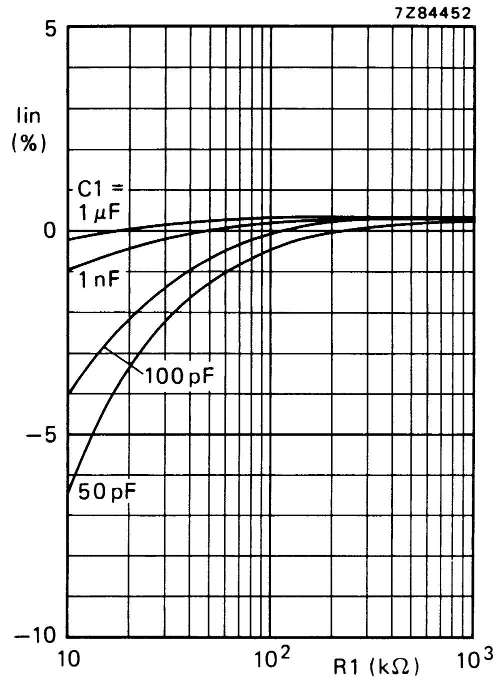


Fig.15 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 10 V.

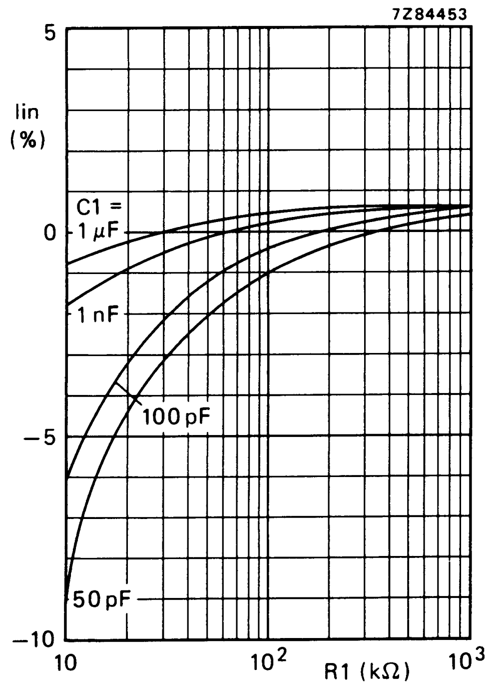


Fig.16 VCO frequency linearity as a function of R1; R2 = ∞; V_{DD} = 15 V.