

## Synthese de fréquence

### 1. Caractérisation du VCO

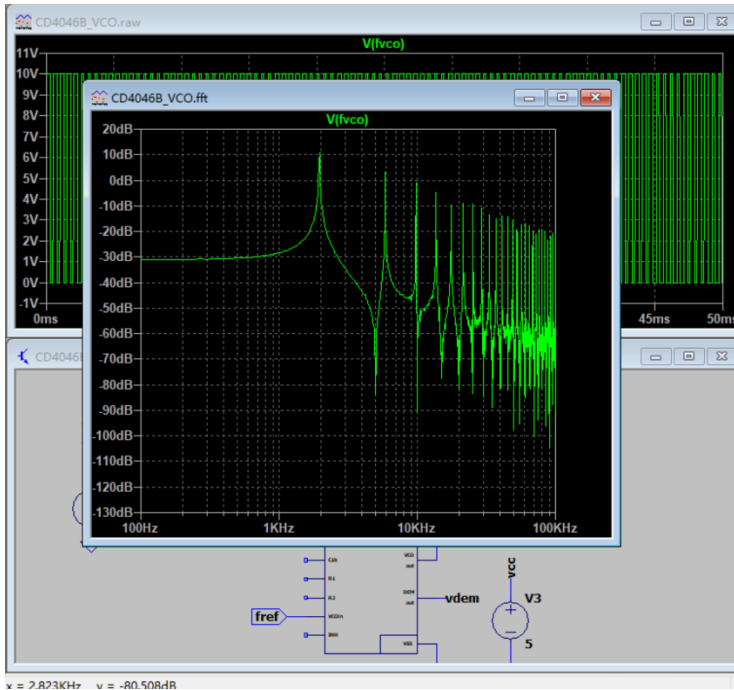
1. Si  $C_1 = 1nF$ ,  $R_1 = 10k\ \Omega$  et  $R_2 = \infty$ , je trouve que  $f_0 \approx 7.8 \times 10^4 Hz$

Alors  $f_{max} = 2 \times f_0 = 1.56 \times 10^5 Hz$ ,  $f_{min} = 0 Hz$

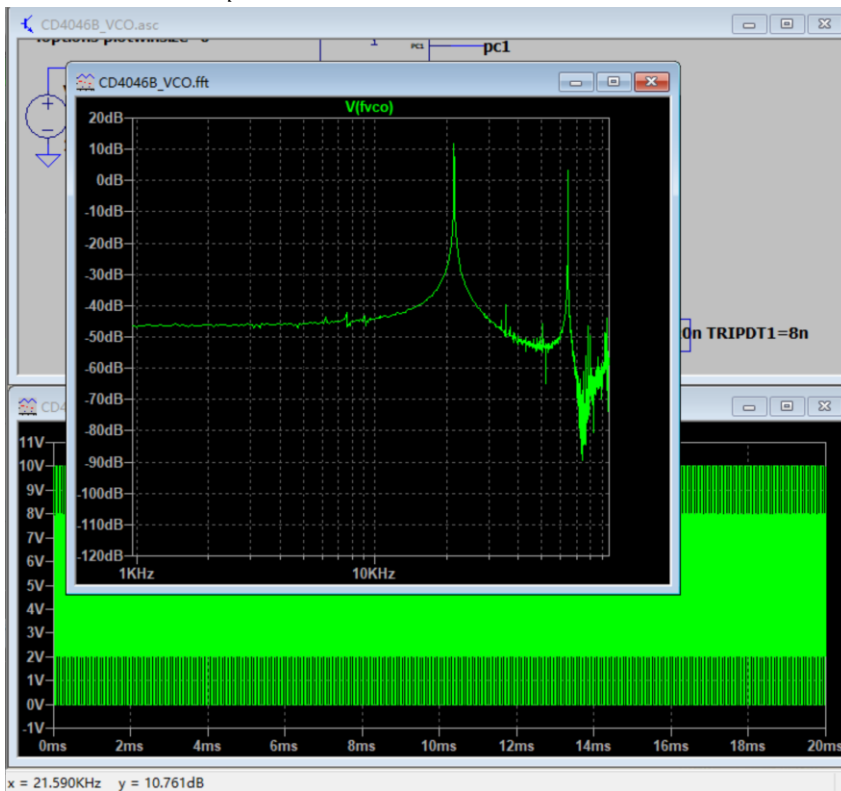
La plage de fonctionnement du VCO est **0~1.56 × 10<sup>5</sup>Hz**

2.

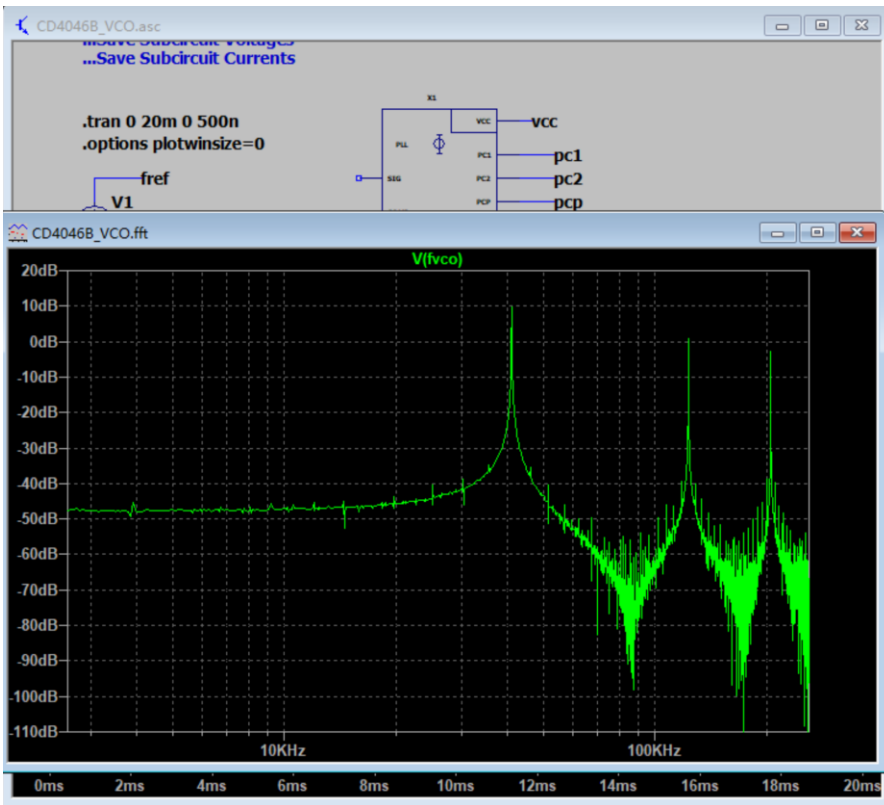
$$V_1 = 1V, f_{harmonique} = 1.965kHz$$



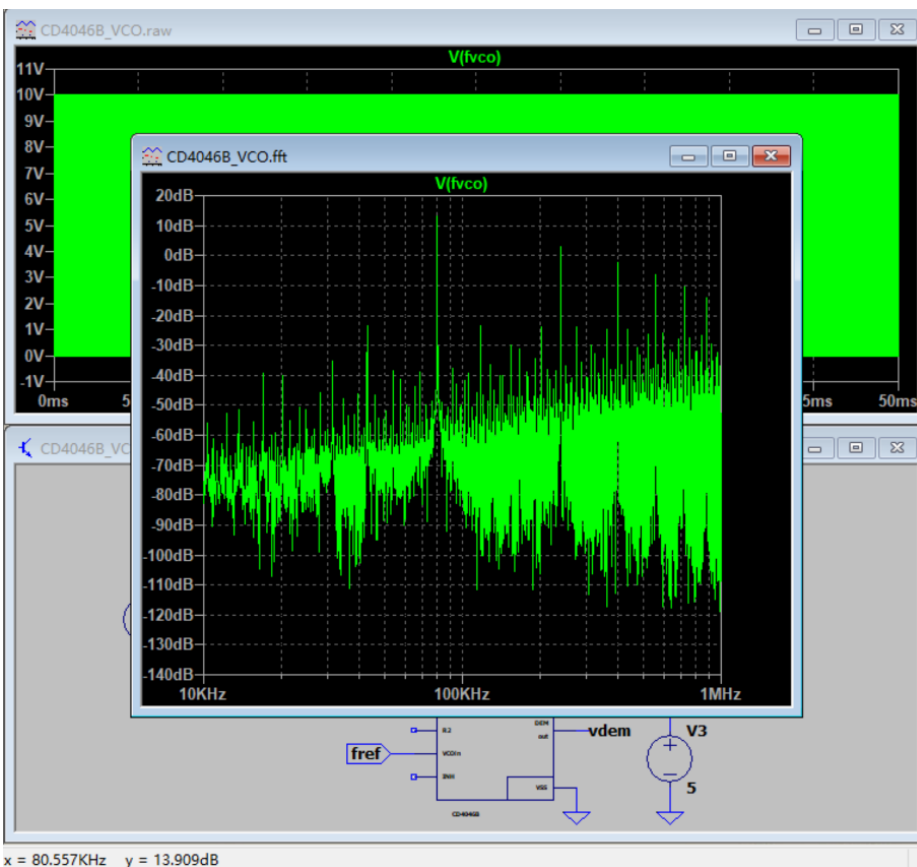
$$V_1 = 2V, f_{harmonique} = 21.3kHz$$



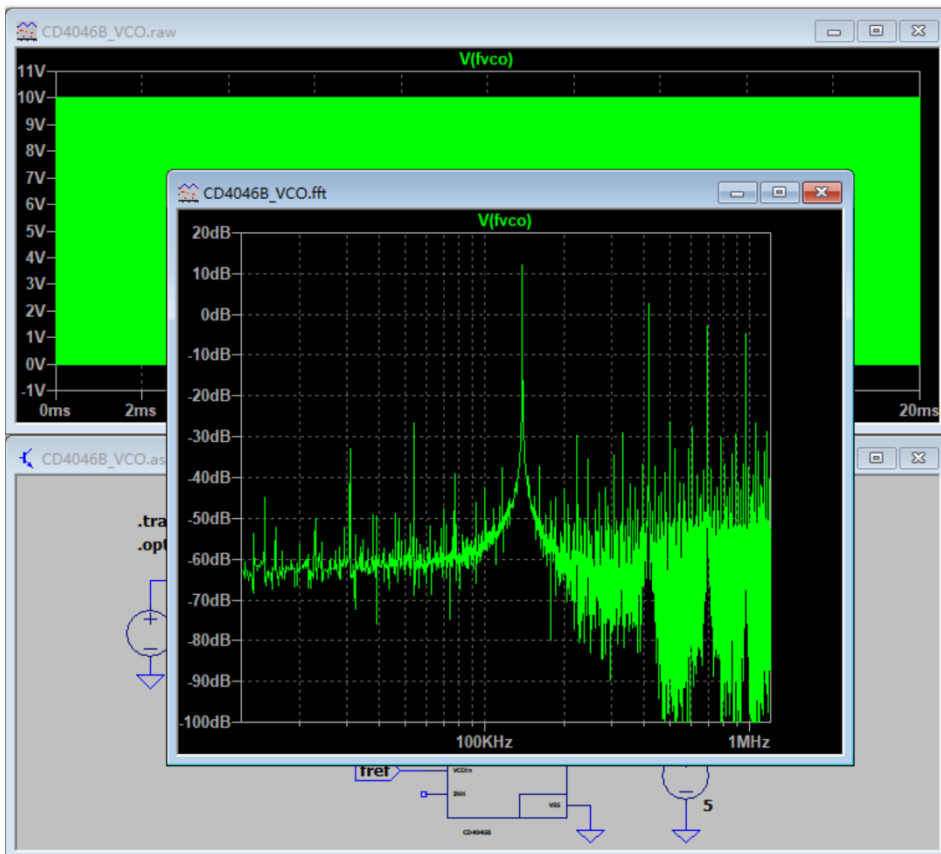
$$V_1 = 3V, f_{harmonic} = 41.3kHz$$



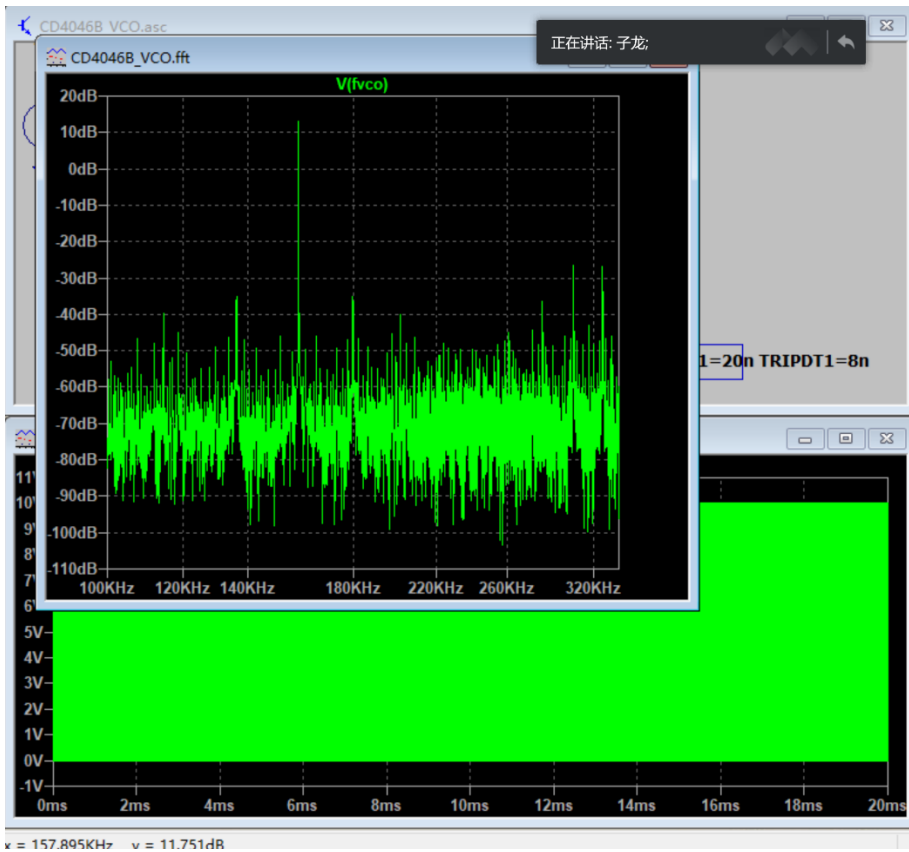
$$V_1 = 5V, f_{harmonic} \approx 80kHz$$



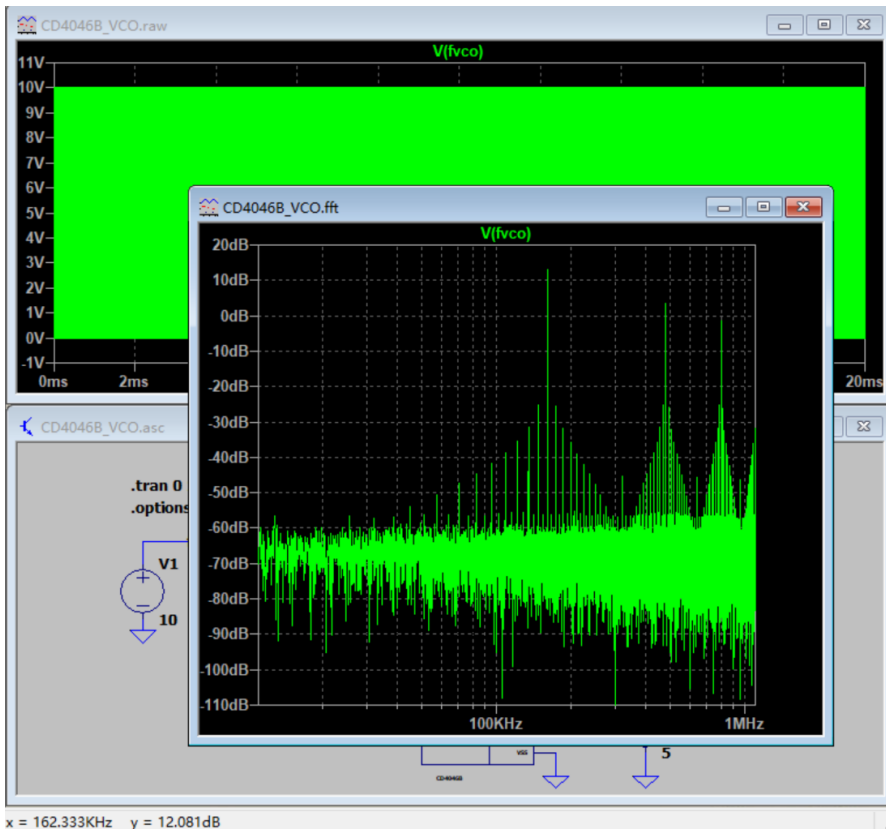
$$V_1 = 8V, f_{harmonic} \approx 138kHz$$



$$V_1 = 9V, f_{harmonic} = 157kHz$$



$$V_1 = 10V, f_{\text{harmonique}} = 160\text{kHz}$$



J'ai constaté une linéarité entre la tension d'entrée et la fréquence de sortie. Notamment entre 1V ~ 9V

$$f_{\text{harmonique}} = 2\text{kHz si } V \leq 1V$$

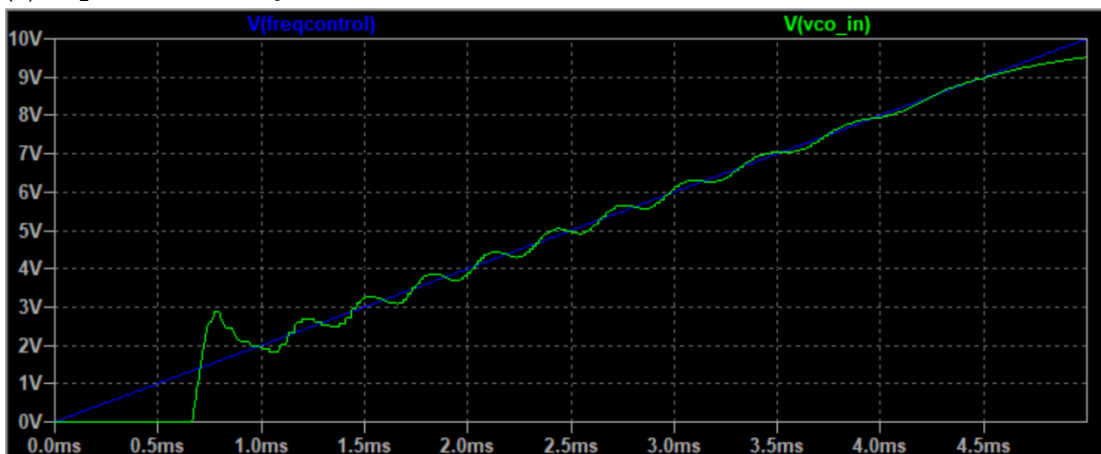
$$f_{\text{haomonique}} = 20k \times (V-1) \text{ si } V \in (1V, 9V)$$

$$f_{\text{harmonique}} = 160\text{kHz si } V \geq 9V$$

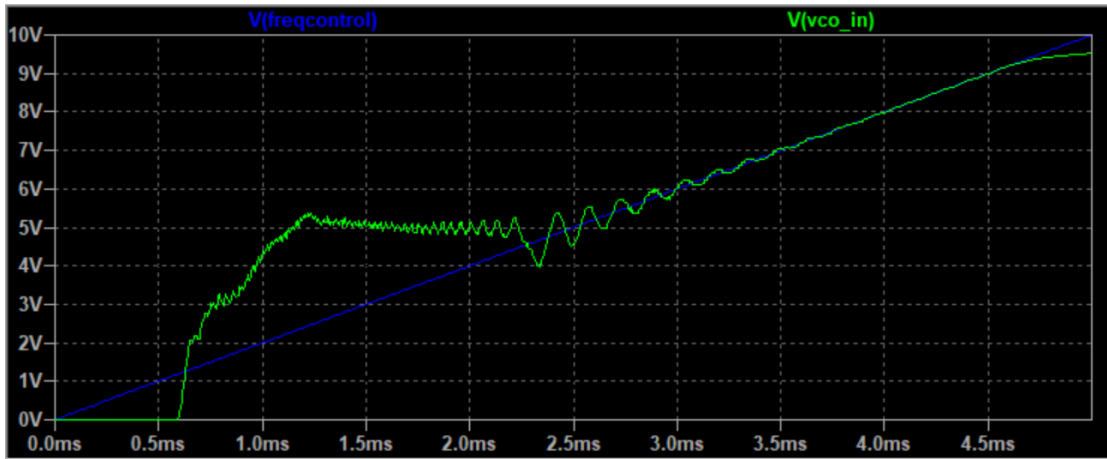
2. Mesure des plages de capture et de verrouillage

3

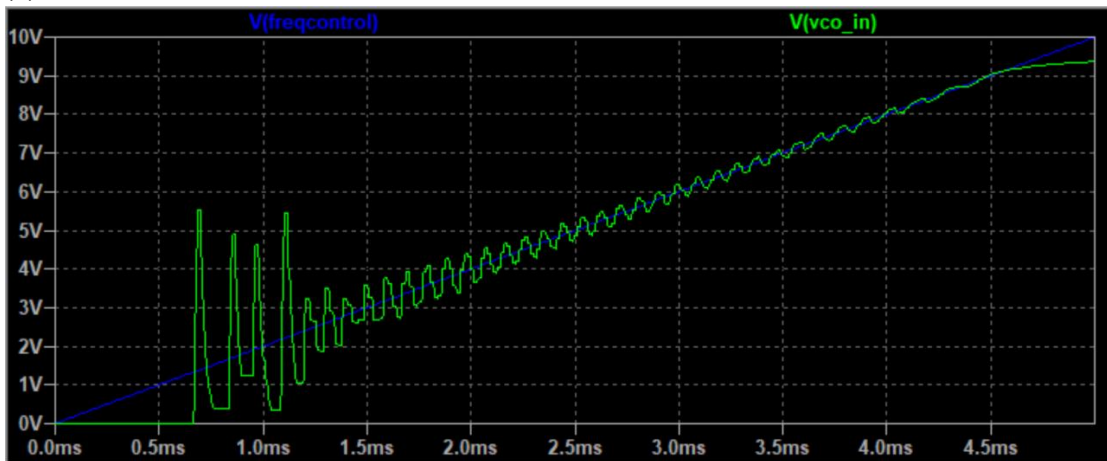
(1):  $C_2 = 100\text{nF}$ , Comparateur = PC2



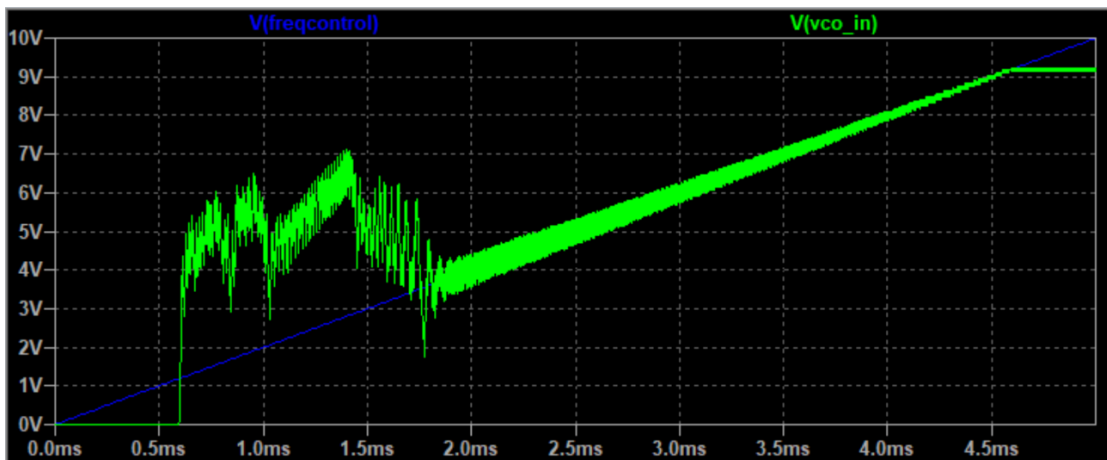
(2):  $C_2 = 100nF$ , Comparateur = PC1



(3) :  $C_2 = 10nF$ , Comparateur = PC2

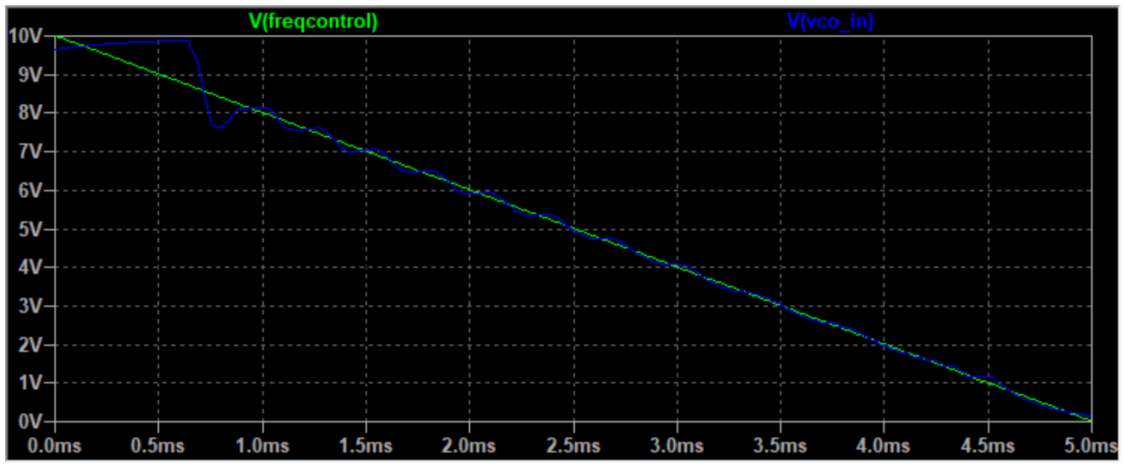


(4) :  $C_2 = 10nF$ , Comparateur = PC1

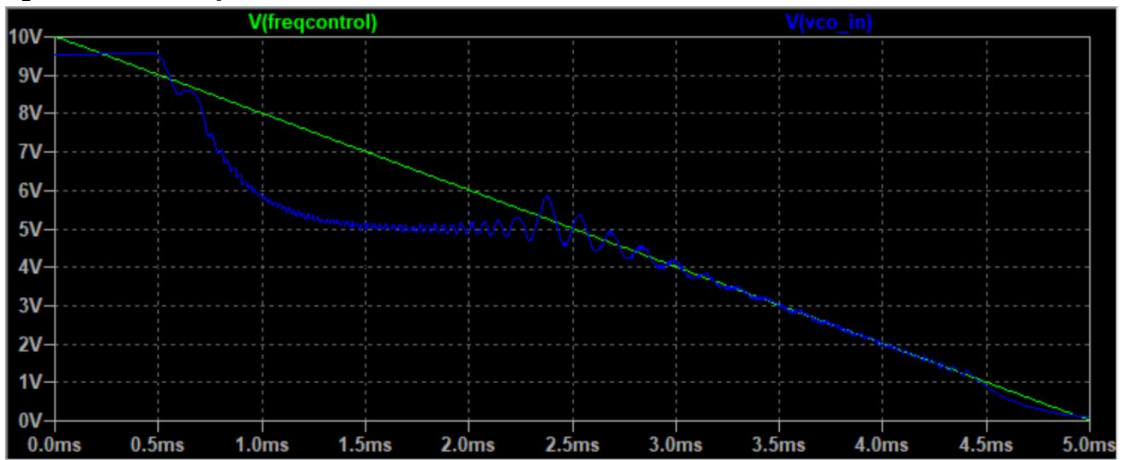


4

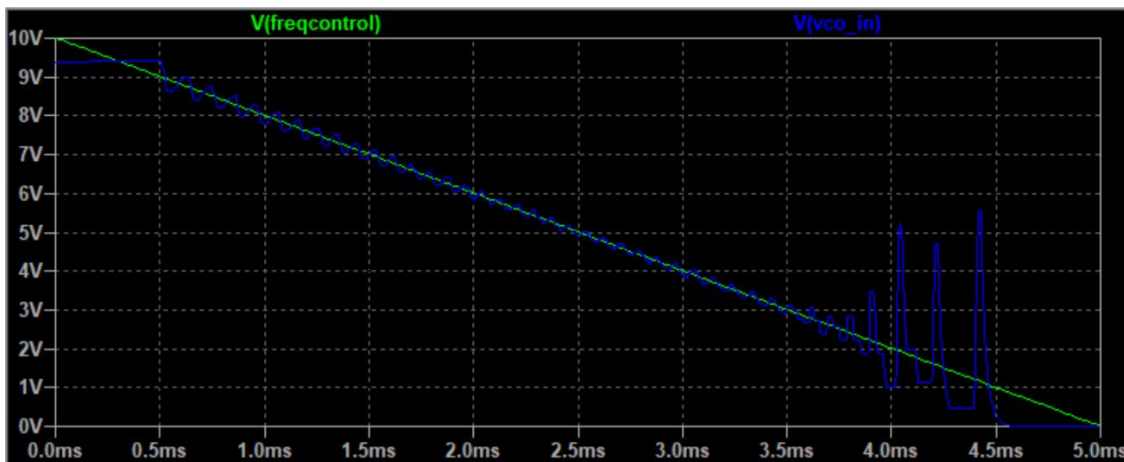
(1) :  $C_2 = 100nF$ , Comparateur = PC2



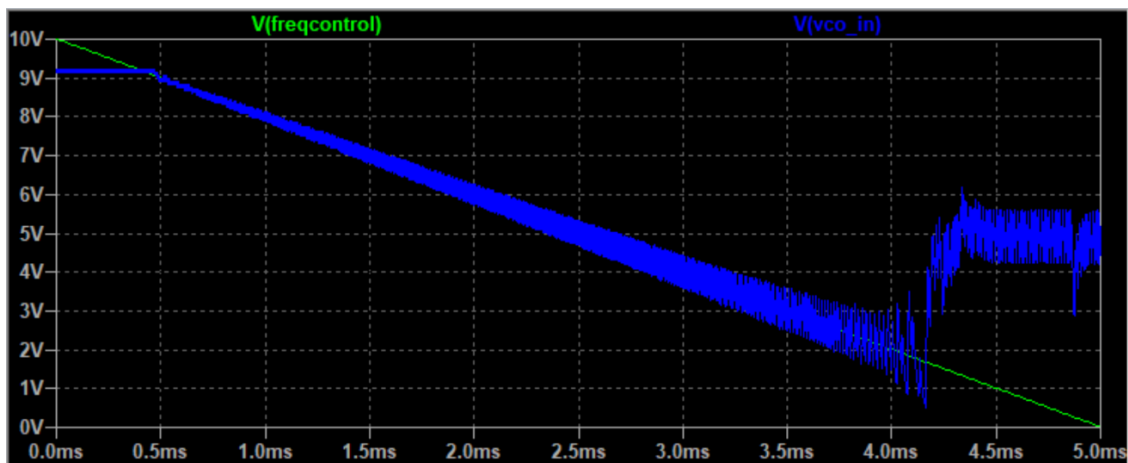
(2)  $C_2 = 100\text{nF}$ , Comparateur = PC1



(3)  $C_2 = 10\text{nF}$ , Comparateur = PC2

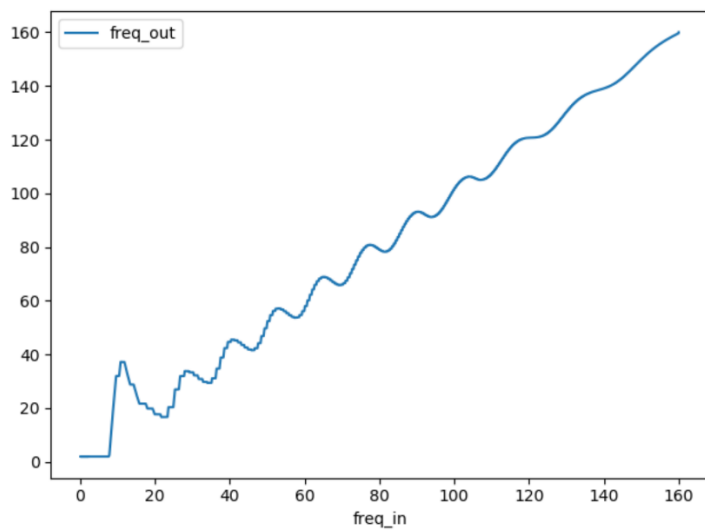


(4)  $C_2 = 10\text{nF}$ , Comparateur = PC1



5.

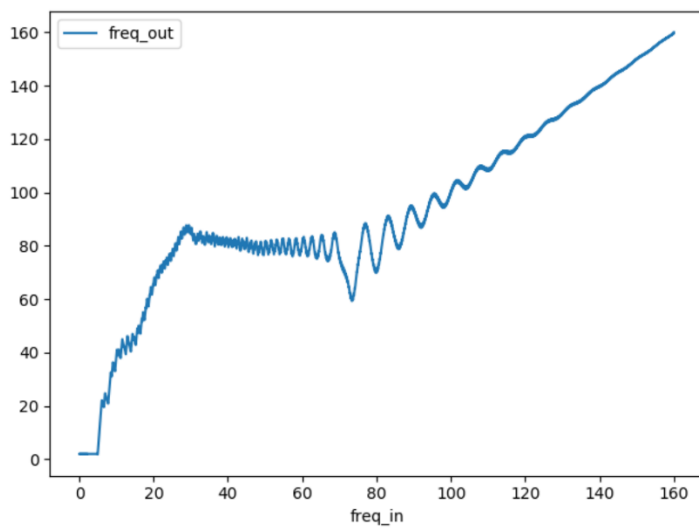
(1) :  $C_2 = 100nF$ , Comparateur = PC2



Plage de verrouillage = 160kHz

Plage de capture = 150kHz

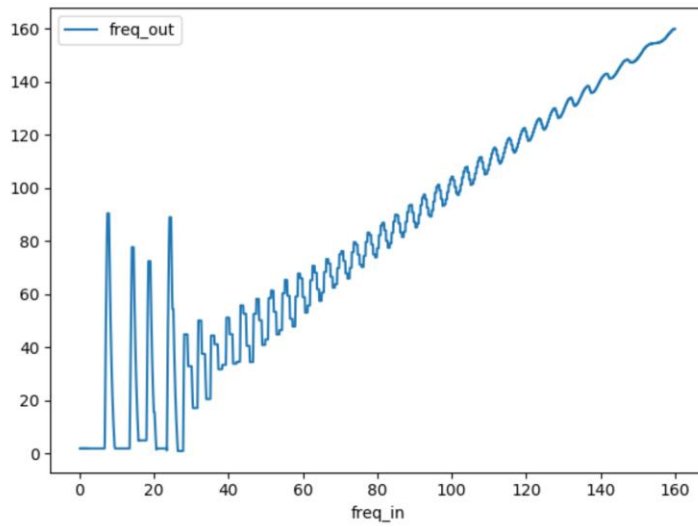
(2) :  $C_2 = 100nF$ , Comparateur = PC1



Plage de verrouillage = 155kHz

Plage de capture = 155kHz

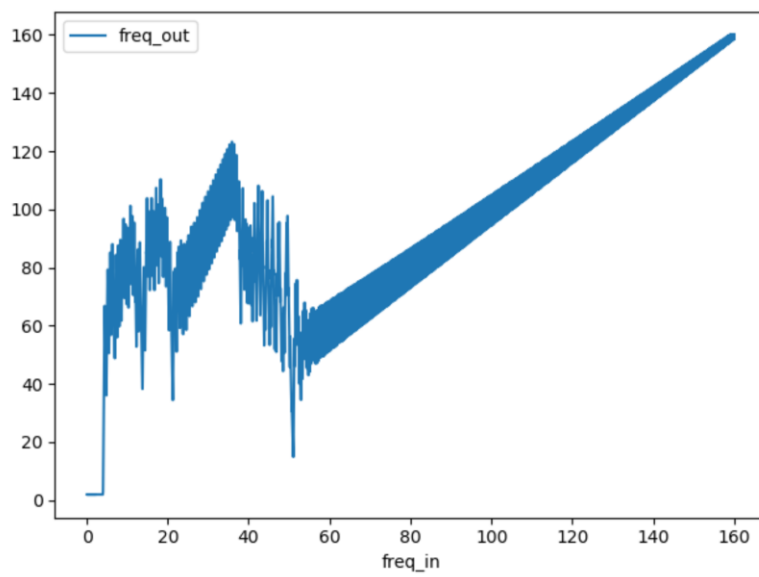
(3) :  $C_2 = 10nF$ , *Comparteur = PC2*



Plage de verrouillage = 155kHz

Plage de capture = 155kHz

(4) :  $C_2 = 10nF$ , *Comparteur = PC1*



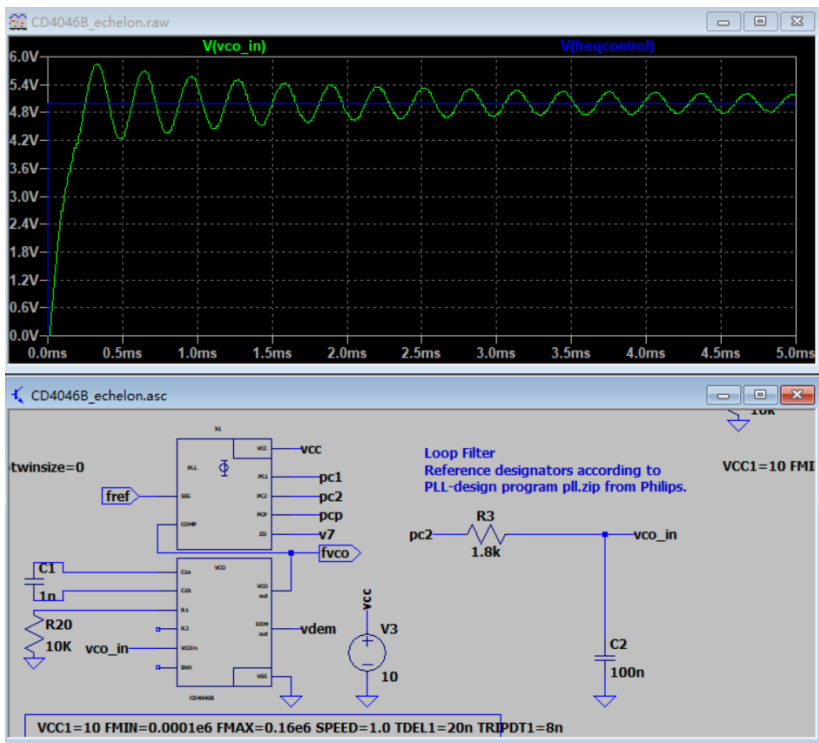
Plage de verrouillage = 155kHz

Plage de capture = 155kHz

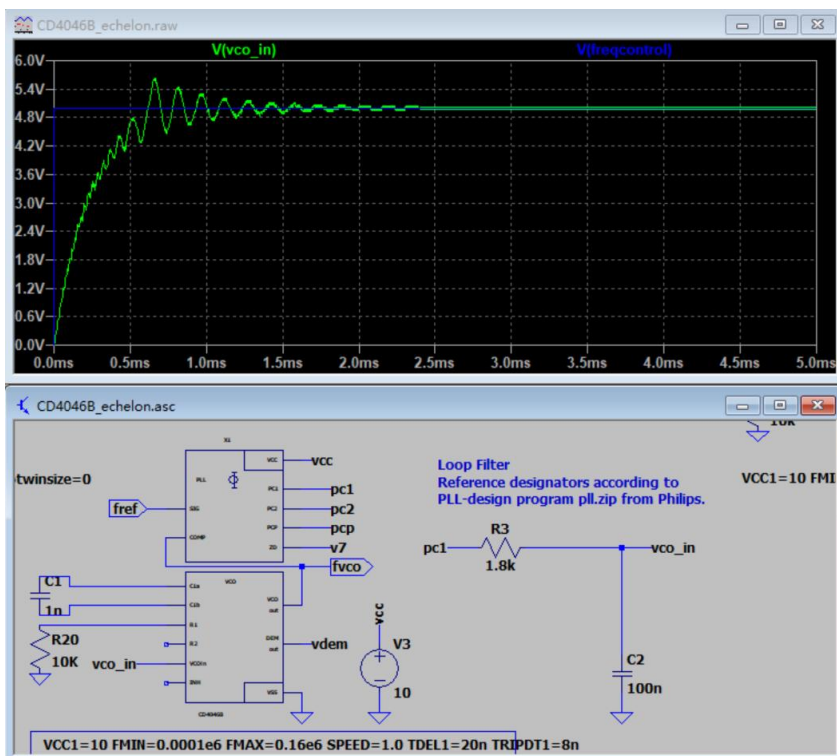


### 3. Réponse de la PLL a un échelon

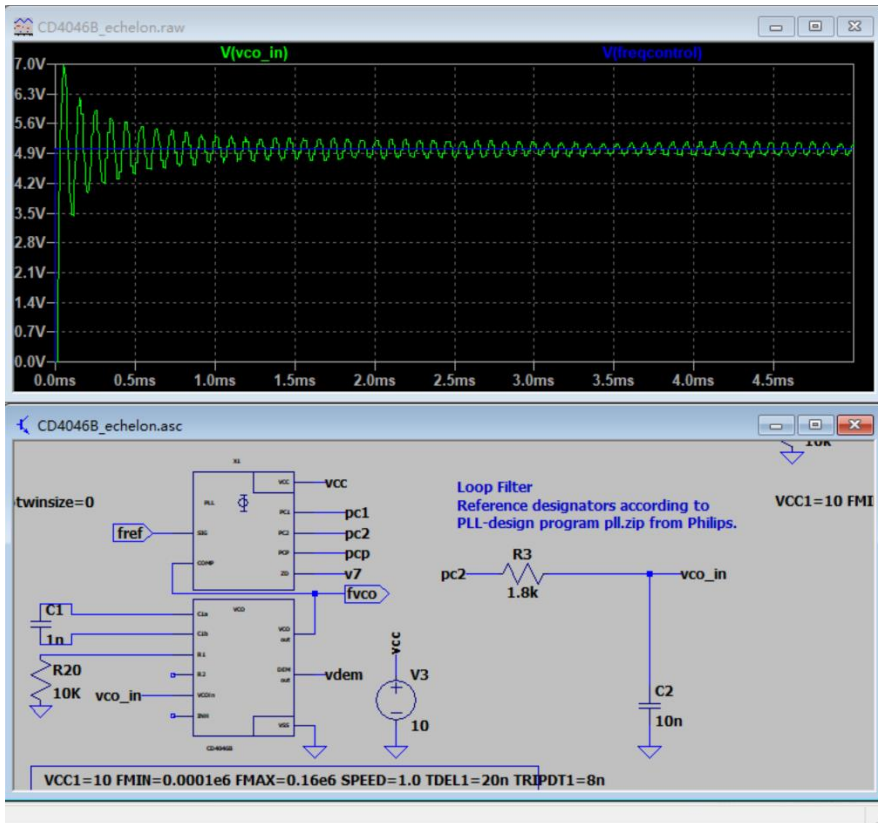
(1) :  $C_2 = 100nF$ , Comparateur = PC2



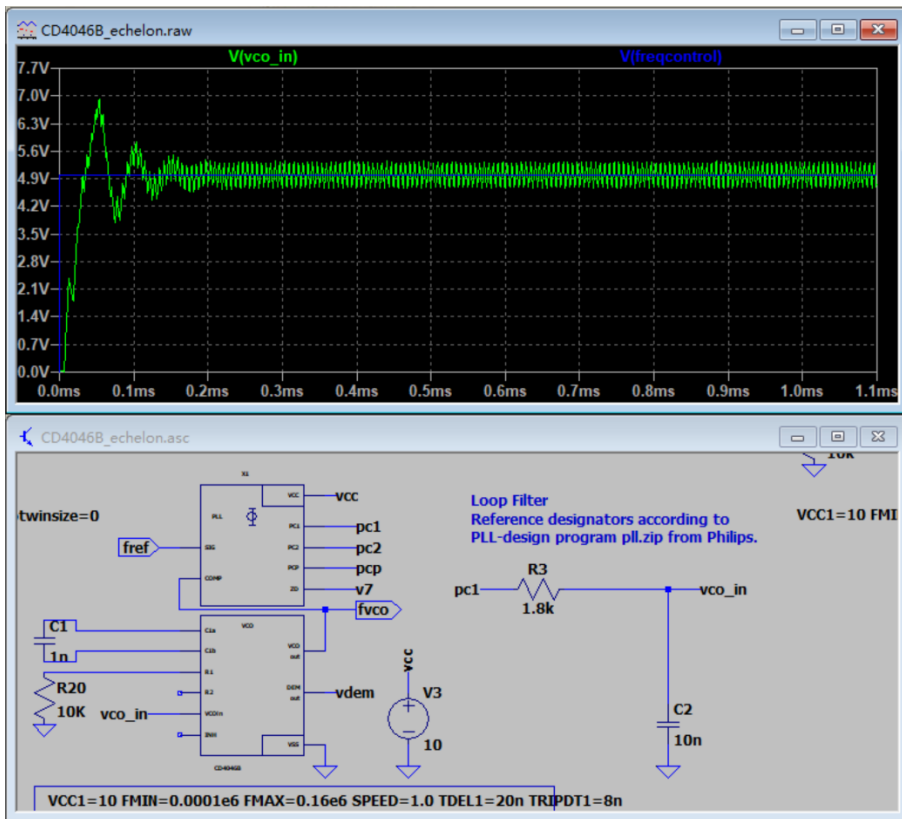
(2) :  $C_2 = 100nF$ , Comparateur = PC1



(3) :  $C_2 = 10nF$ , Comparateur = PC2



(4) :  $C_2 = 10nF$ , Comparateur = PC1



2.

(1) :  $C_2 = 100nF$ , *Compareur = PC2*

$$t_{90\%} = 0.25ms$$

(2) :  $C_2 = 100nF$ , *Compareur = PC1*

$$t_{90\%} = 0.5ms$$

(3) :  $C_2 = 10nF$ , *Compareur = PC2*

$$t_{90\%} = 0.03ms$$

(4) :  $C_2 = 10nF$ , *Compareur = PC1*

$$t_{90\%} = 0.03ms$$

3.

Le temps est plus court si on prend une capacité plus petite.