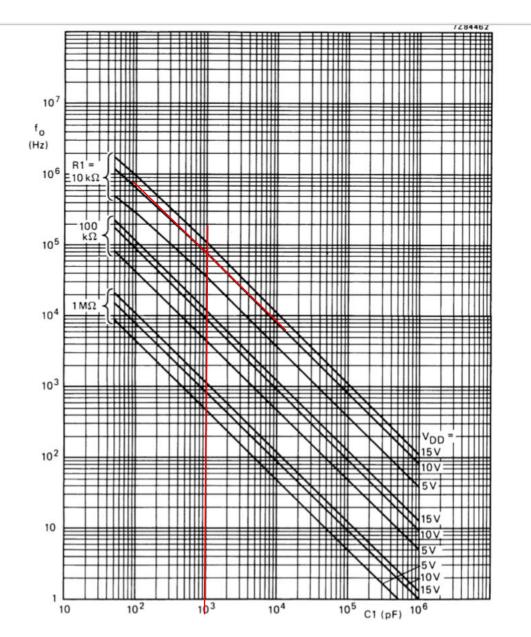
Étude de la PLL CD4046B

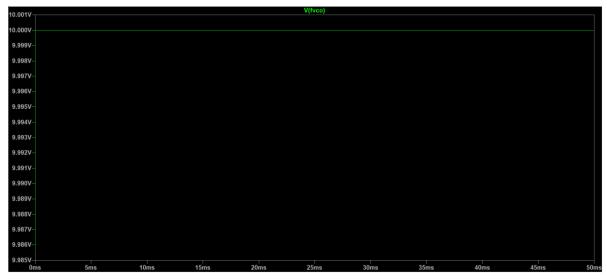
1 Caractérisation du VCO

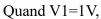
1. C1=1nF, R1=10kΩ, R2 infinie, donc on choisit la figure 7

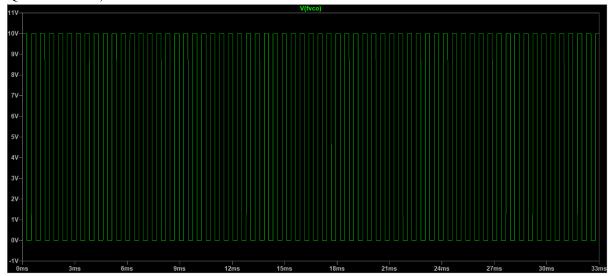


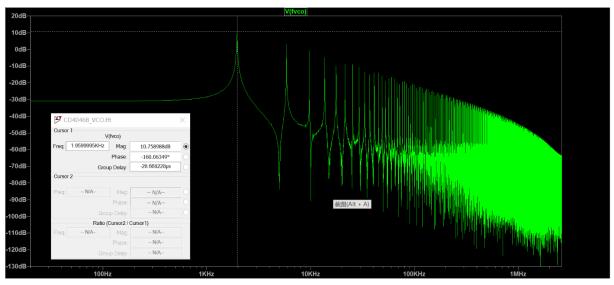
On peut voir que f0 = 75 kHz, fmax = 2 f0 = 150 kHz, le plage de fonctionnement 150 kHz

2. Quand V1=0V,

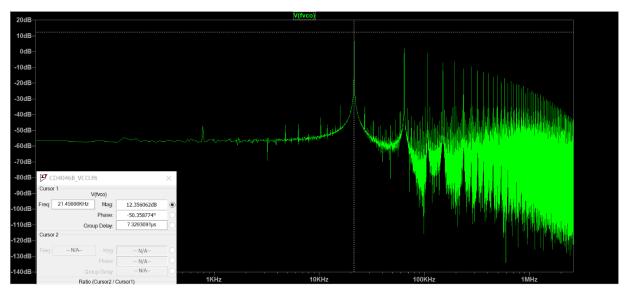




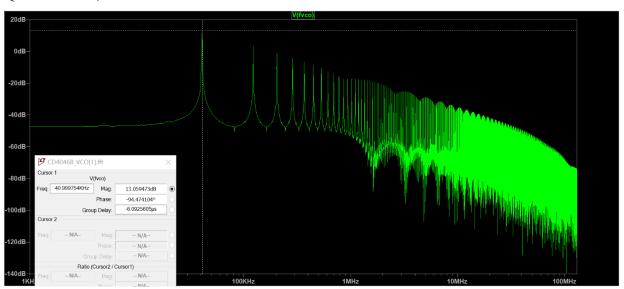




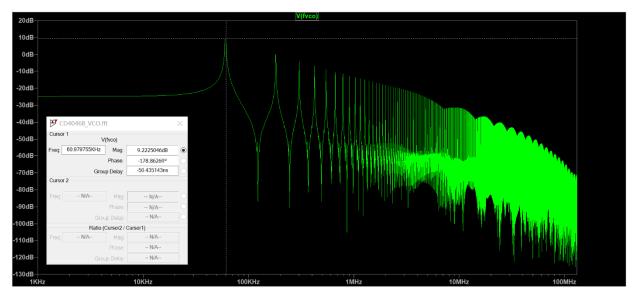
f = 1.96kHz, G = 10.76dBQuand V1=2V,



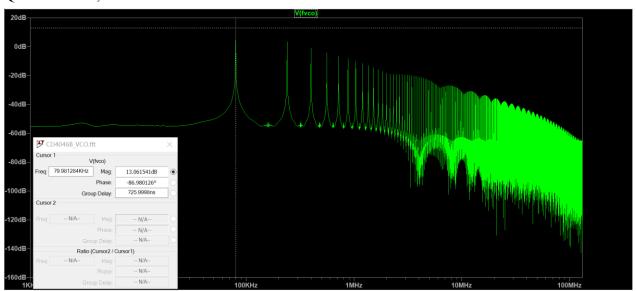
f = 21.46kHz, G = 12.36dBQuand V1=3V,



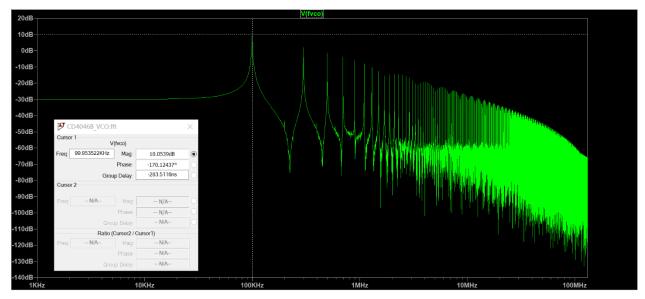
f = 41.00kHz, G = 13.06dBQuand V1=4V,



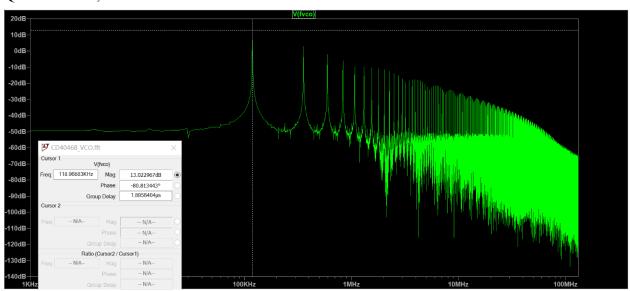
f = 60.98kHz, G = 9.22dBQuand V1=5V,



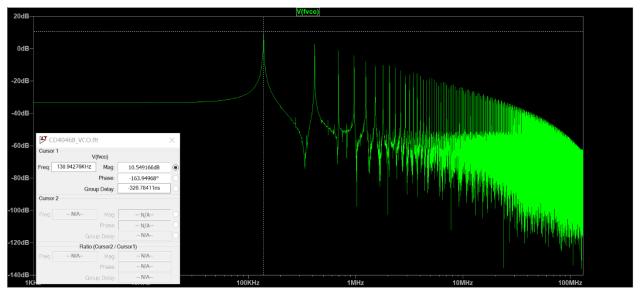
f = 79.98kHz, G = 13.06dBQuand V1=6V,



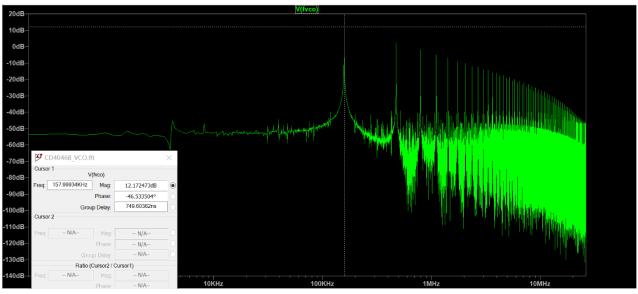
f = 99.95kHz, G = 10.05dBQuand V1=7V,



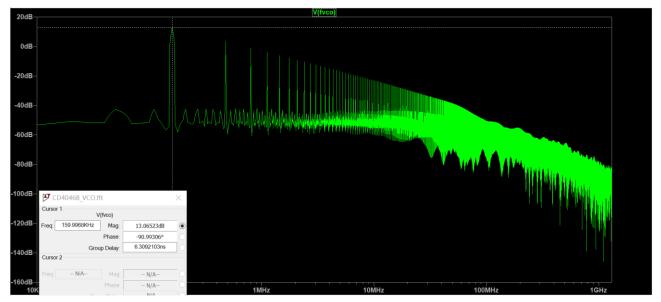
f = 118.97kHz, G = 13.02dBQuand V1=8V,



f = 138.94kHz, G = 10.55dBQuand V1=9V,

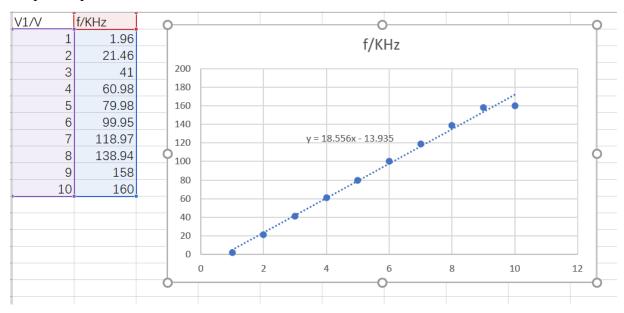


f = 158.00kHz, G = 12.17dBQuand V1=10V,



f = 160.00kHz, G = 13.07dB

On peut exprimer la relation entre V1 et f dans Excel

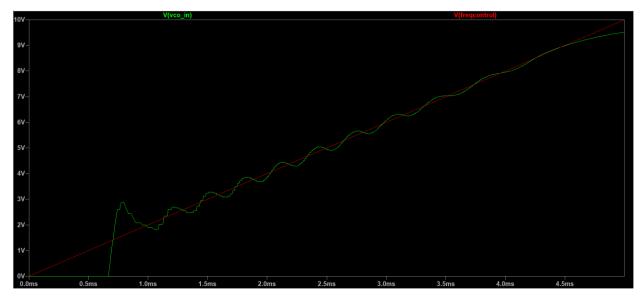


Quand V1 ϵ [1,9], la relation est linéaire. La relation est :f=18.556V-13.935

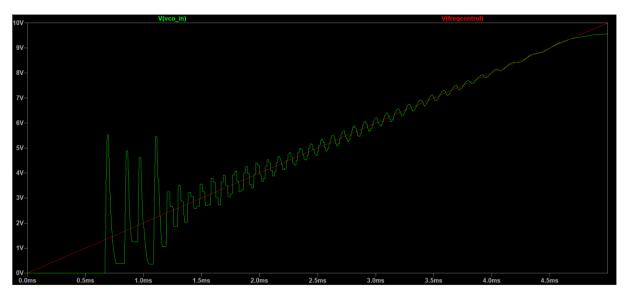
Quand V1 ϵ [0,1], la relation est : f=1.96V Quand V1 ϵ [0,1], la relation est : f=2V+140

2 Mesure des plages de capture et de verrouillage

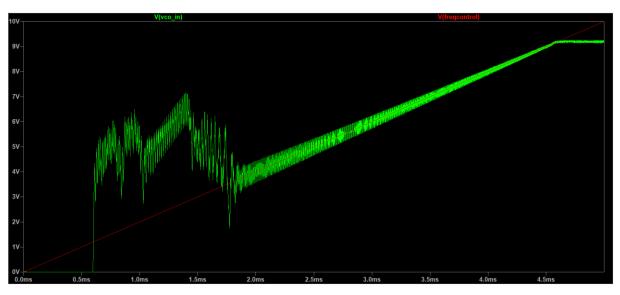
3. PC2 : C2 = 100nF



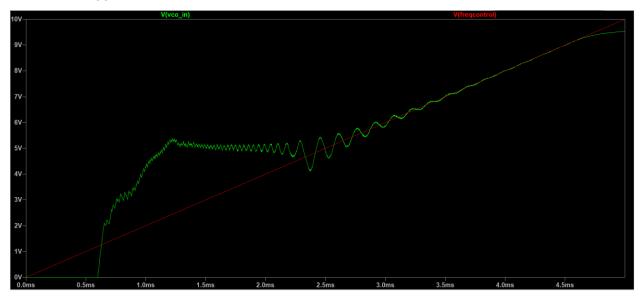
PC2 : C2 = 10nF



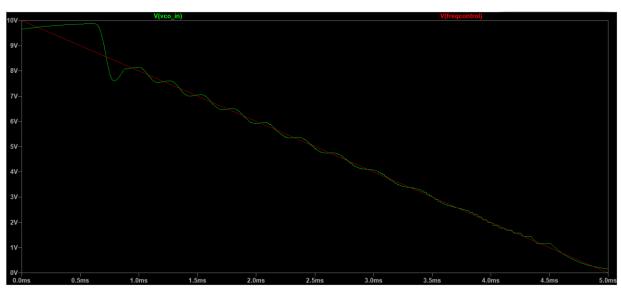
PC1 : C2 = 10nF



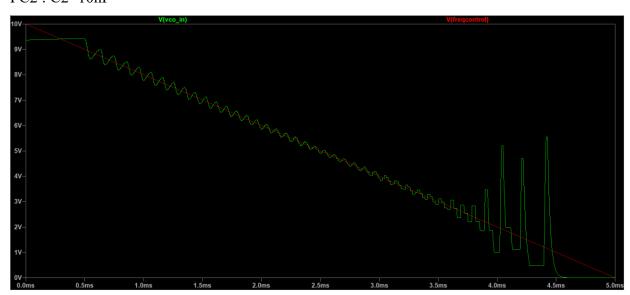
PC1:C2 = 100nF



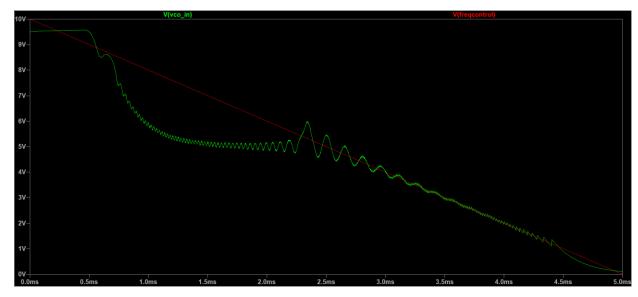
4. PC2 : C2 = 100nF



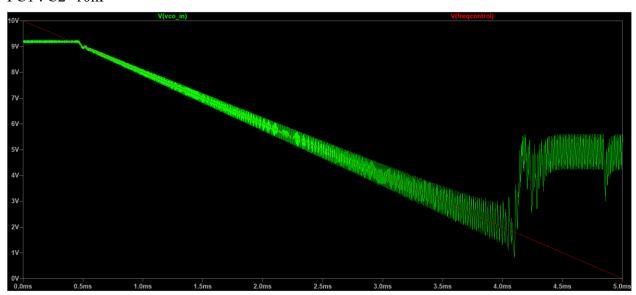
PC2: C2=10nF



PC1: C2=100nF



PC1: C2=10nF

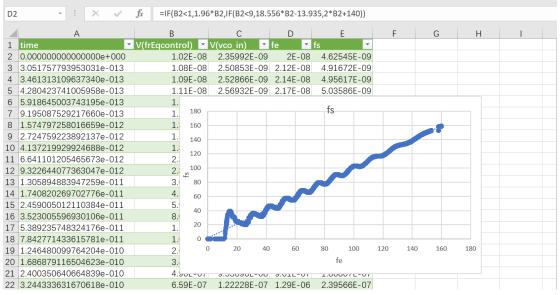


5. D'après la question 2 de partie 1,

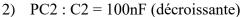
Quand $V1\epsilon[1,9]$, la relation est linéaire. La relation est :f=18.556V-13.935

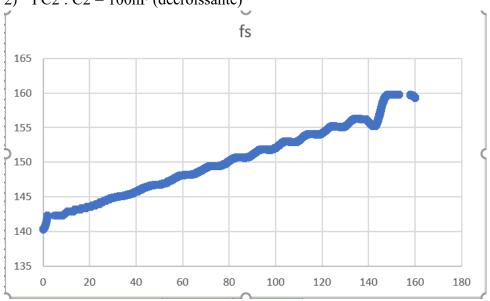
Quand V1 ϵ [0,1], la relation est : f=1.96V Quand V1 ϵ [0,1], la relation est : f=2V+140

1) PC2 : C2 = 100nF (croissante)



f1=11.60KHz, f2=160.00KHz



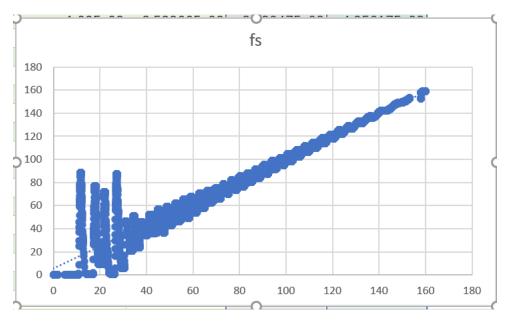


f1=0KHz,f2=146.50KHz

donc, la plage de capture est : 11.60KHz-146.50KHz

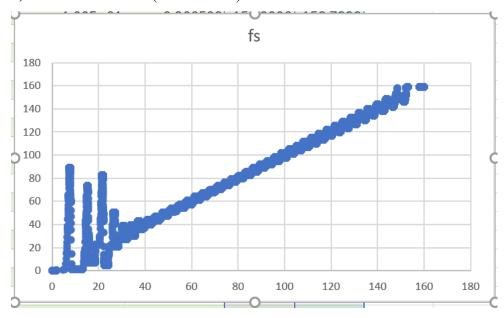
La plage de verrouillage : 0-160.00kHz

3) PC2: C2 = 10nF (croissante)



f1=13.49KHz, f2=160.00KHz

4) PC2 : C2 = 10nF (décroissante)

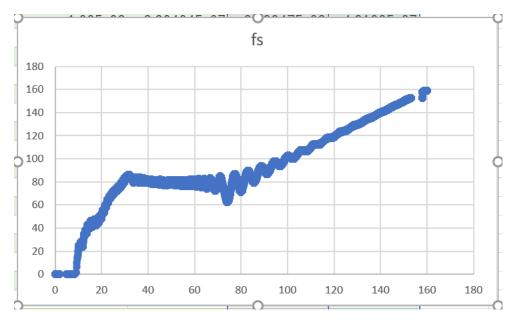


f1=4.80KHz, f2=152.21KHz

donc, la plage de capture est : 13.49KHz-152.21KHz

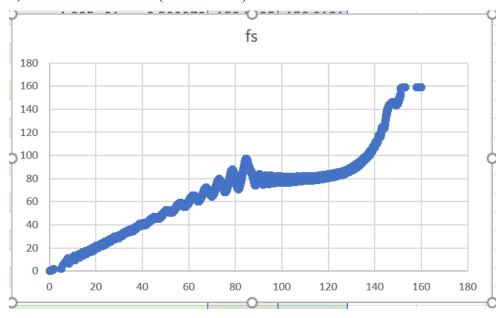
La plage de verrouillage : 4.80-160.00kHz

5) PC1 : C2 = 100nF (croissante)



f1=8.88KHz, f2=160.00KHz

6) PC1 : C2 = 100nF (décroissante)

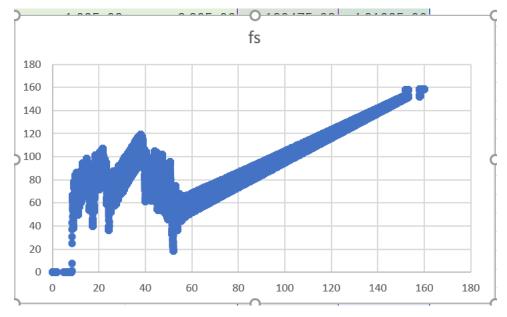


f1=0KHz, f2=151.17KHz

donc, la plage de capture est : 8.88KHz-151.17KHz

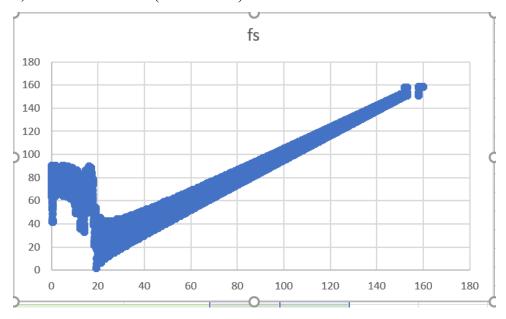
La plage de verrouillage : 0-160.00kHz

7) PC1 : C2 = 10nF (croissante)



f1=8.15KHz, f2=159.98KHz

8) PC1: C2 = 10nF (décroissante)



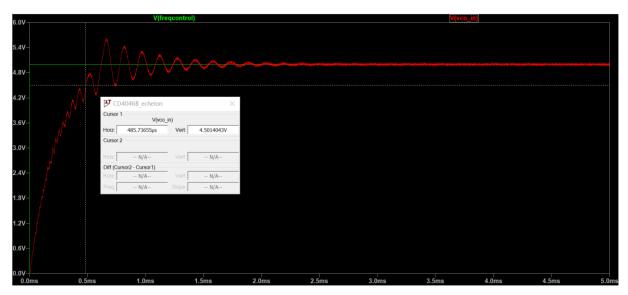
f1=0KHz, f2=151.85KHz

donc, la plage de capture est : 8.15KHz-151.85KHz

La plage de verrouillage : 0-151.85kHz

3 Réponse de la PLL à un échelon

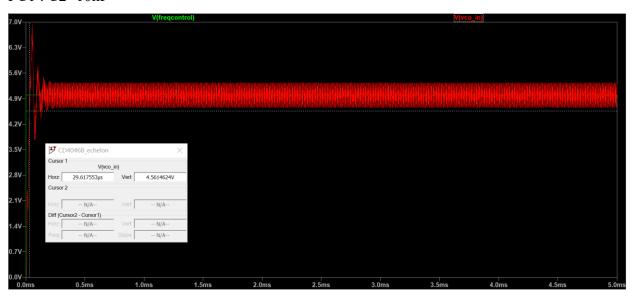
1&2. PC1 : C2=100nF



V(freqcontrol) = 5V, 0.9* V(freqcontrol) = 4.5V

le temps pour atteindre 90% est $485.74 \mu s$

PC1:C2=10nF



V(freqcontrol) = 5V, 0.9* V(freqcontrol) = 4.5V

le temps pour atteindre 90% est 29.62µs

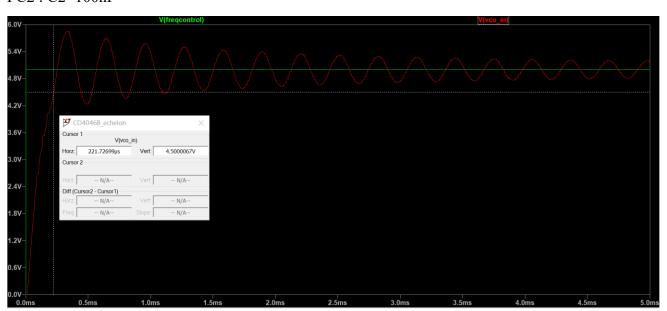
PC2: C2=10nF



V(freqcontrol) = 5V, 0.9* V(freqcontrol) = 4.5V

le temps pour atteindre 90% est 27.59µs

PC2: C2=100nF



$$V(freqcontrol) = 5V, 0.9* V(freqcontrol) = 4.5V$$

le temps pour atteindre 90% est 221.73µs

3. Temps caractéristiques : $\tau = RC$ Quand C2=10nF, R3=1.8KHz, $\tau = 18\mu s$ D'après la question précétente, PC1, $\tau = 29.62\mu s$ PC2, $\tau = 27.59\mu s$ Quand C2=100nF, R3=1.8KHz, $\tau = 180\mu s$ D'après la question précétente,

PC1,
$$\tau = 485.74\mu s$$
 PC2, $\tau = 227.31\mu s$