

Electronique

Etude de la PLL CD4046B

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1. Caractérisation du VCO

1. D'après la figure 7 dans le document technique, on trouve que

$$f_0 = 80kHz$$

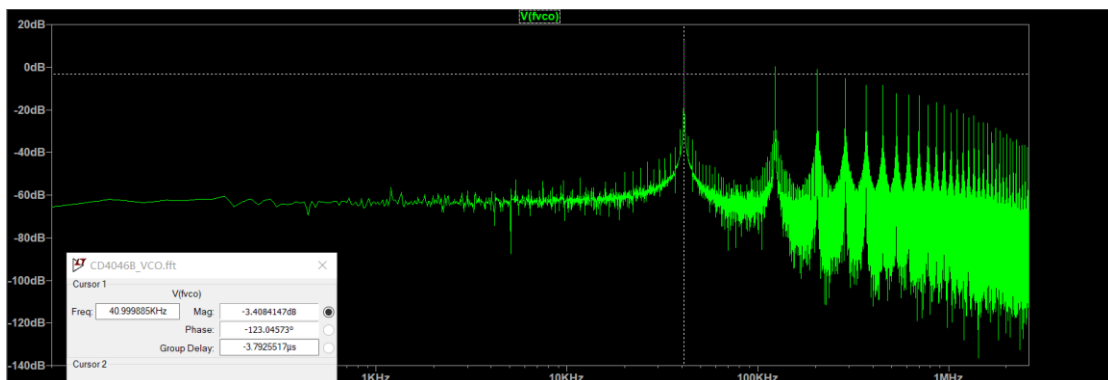
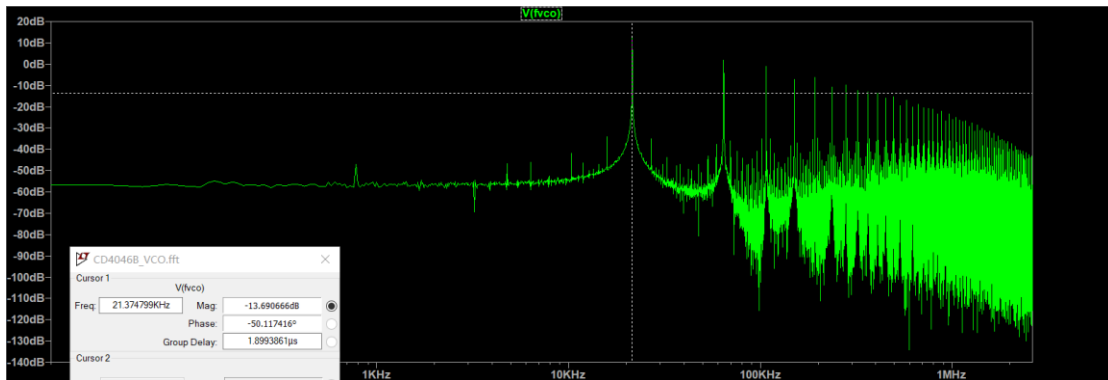
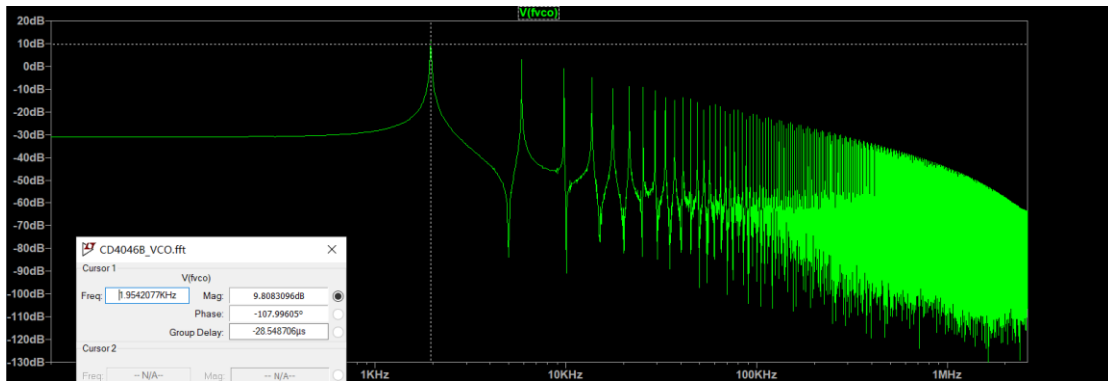
Alors on a

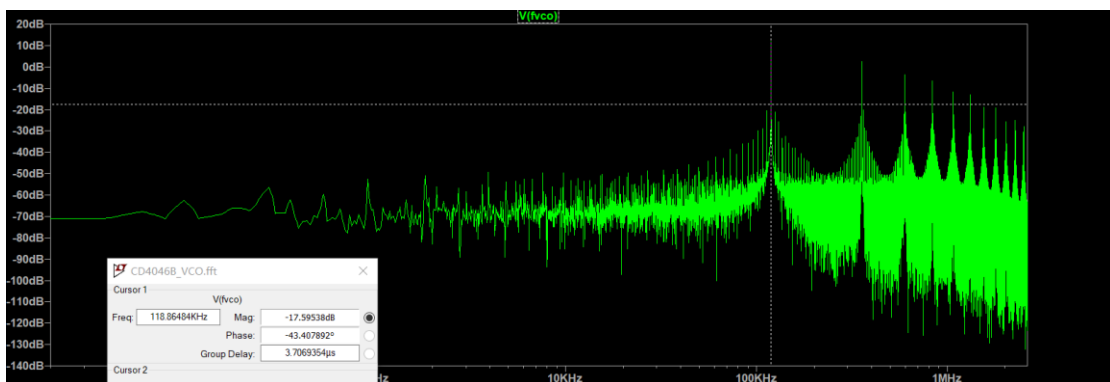
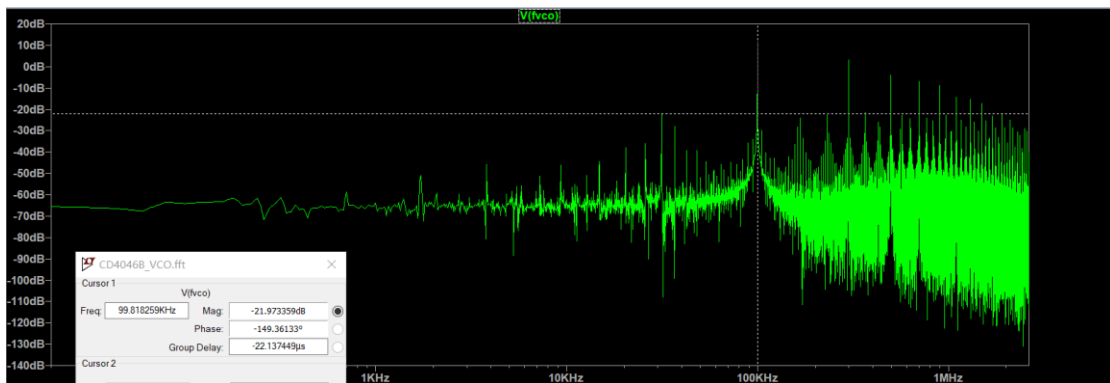
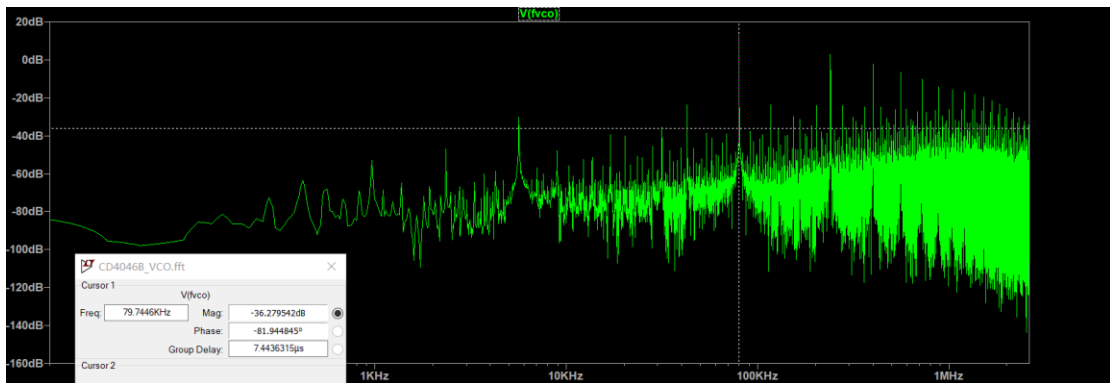
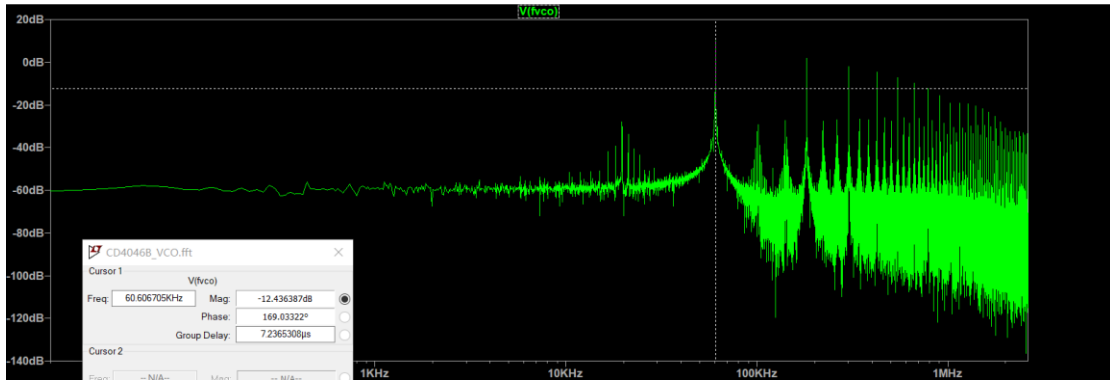
$$f_{max} = 2f_0 = 160kHz$$

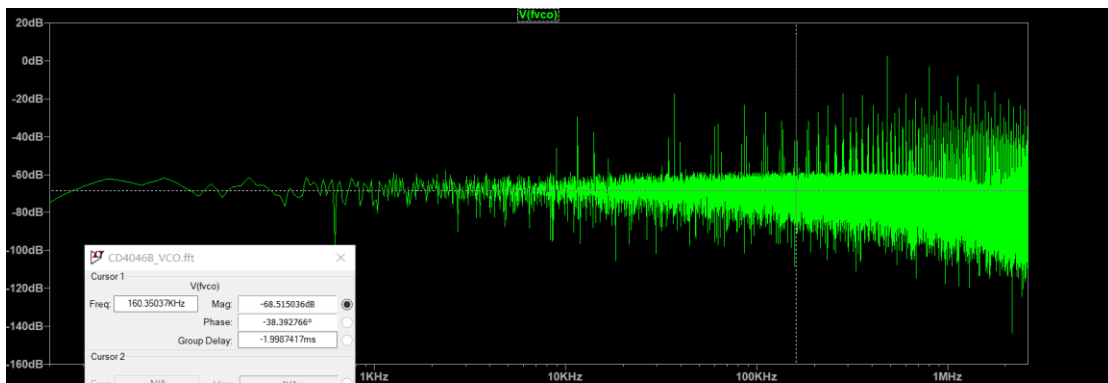
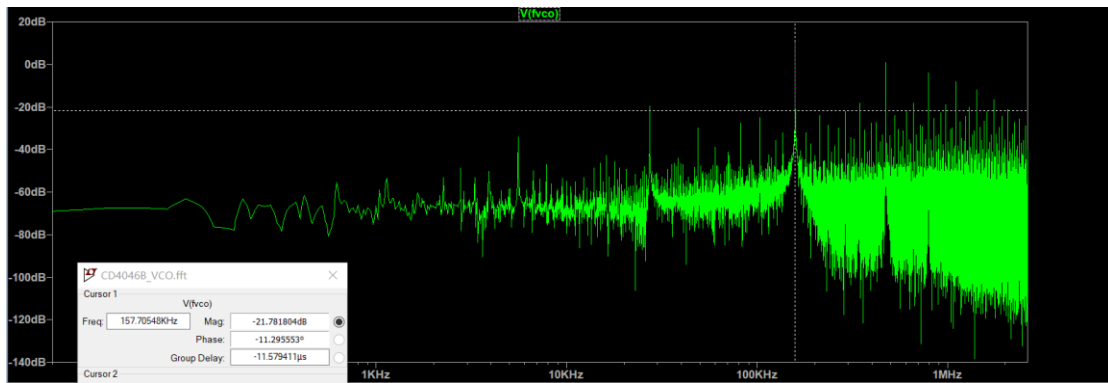
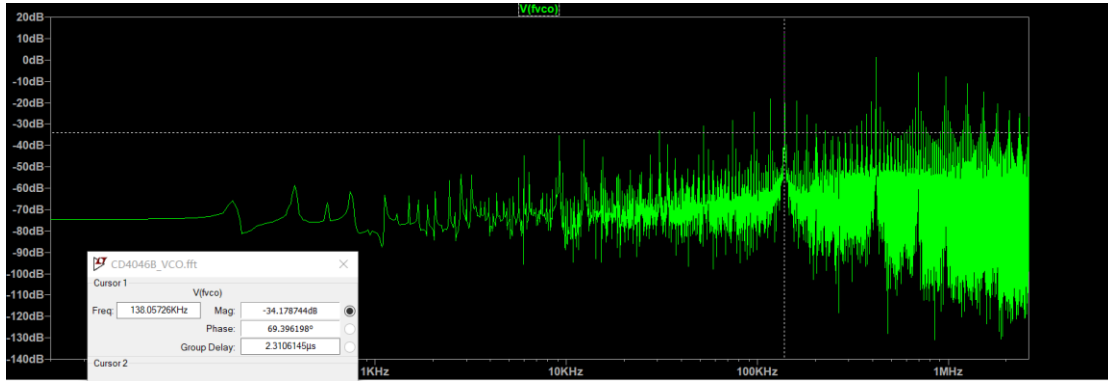
2. On mesurera la fréquence du signal f_{vco} en sortie du VCO :

On prendra pour la tension d'entrée V_1 des valeurs de 0 à 10 V par pas de 1 V.

[$V_1=1,2,3...10V$]

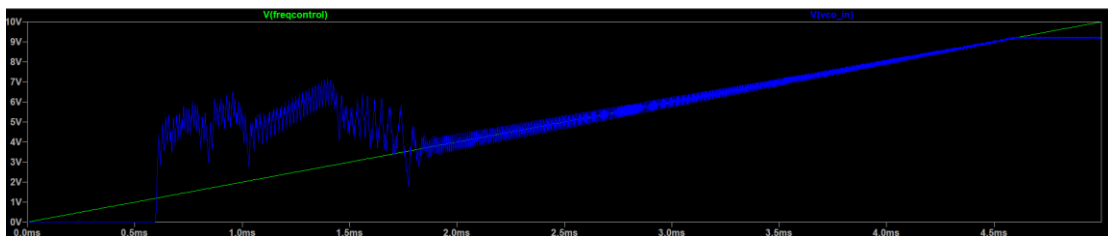




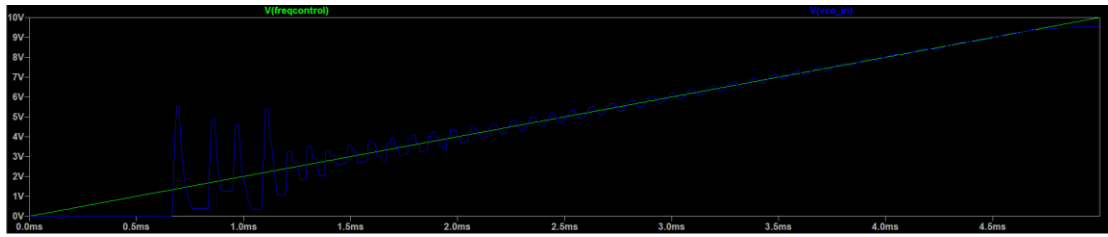


2. Mesure des plages de capture et de verrouillage

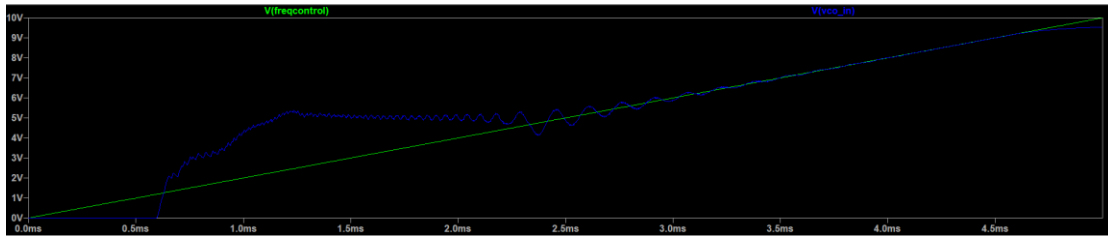
3. $PC_1, C_2 = 10nF$



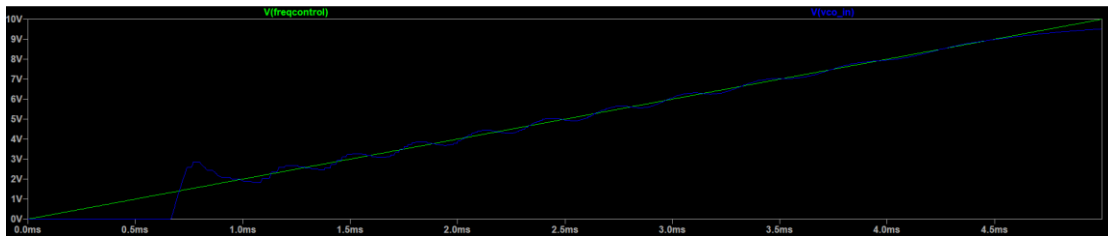
PC2, $C_2 = 10nF$



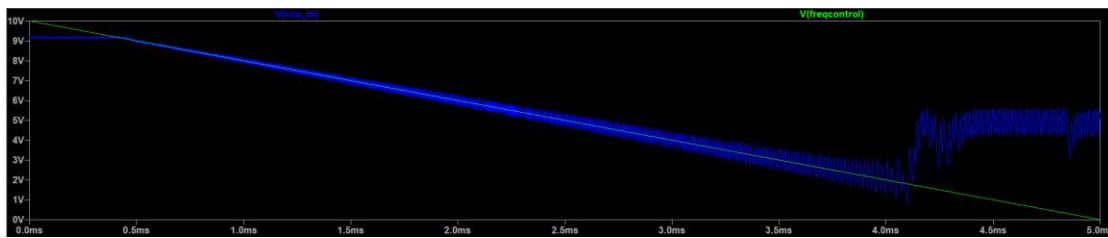
PC1, $C_2 = 100nF$



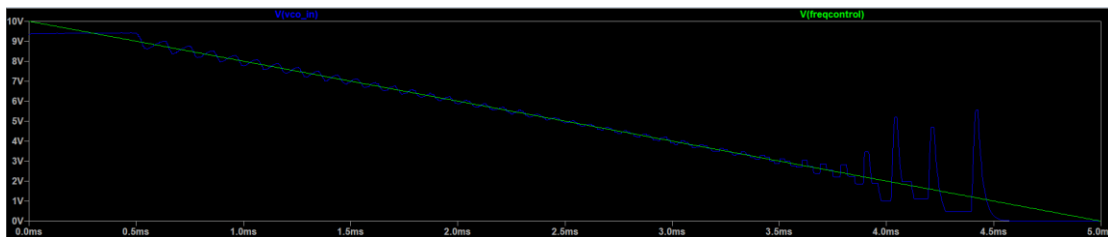
PC2, $C_2 = 100nF$



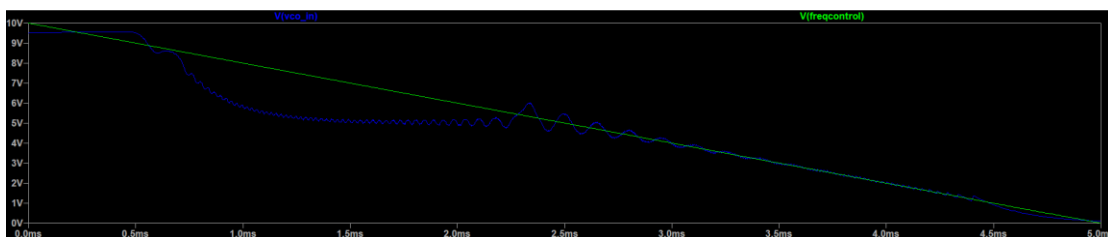
4. PC1, $C_2 = 10nF$



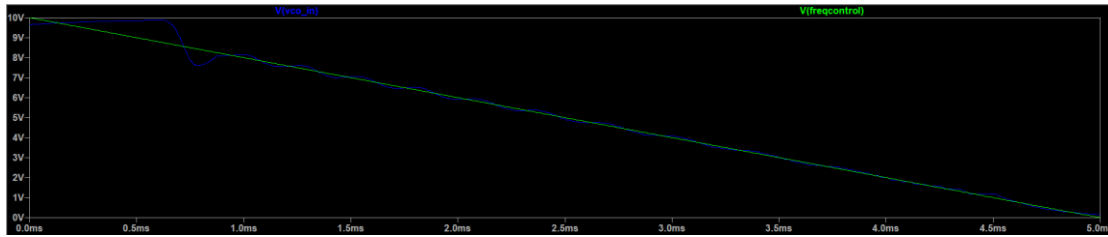
PC2, $C_2 = 10nF$



PC1, $C_2 = 100nF$



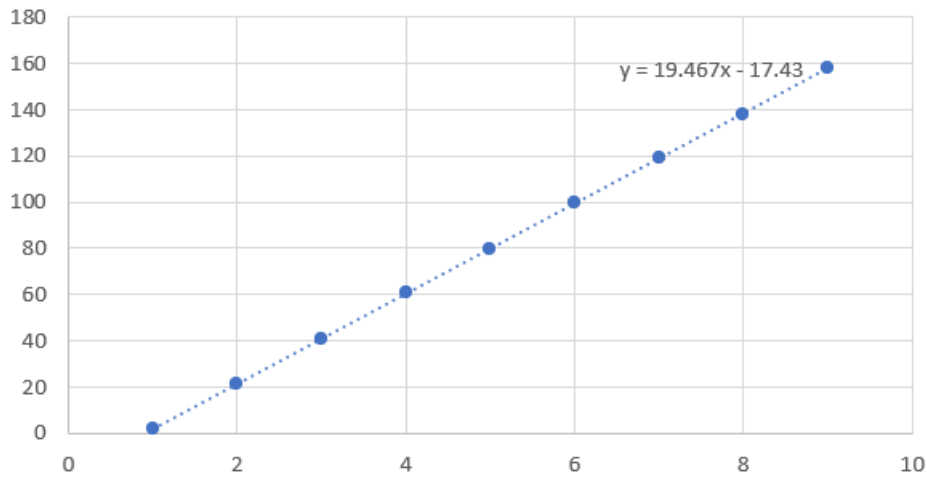
PC2, $C_2 = 100nF$



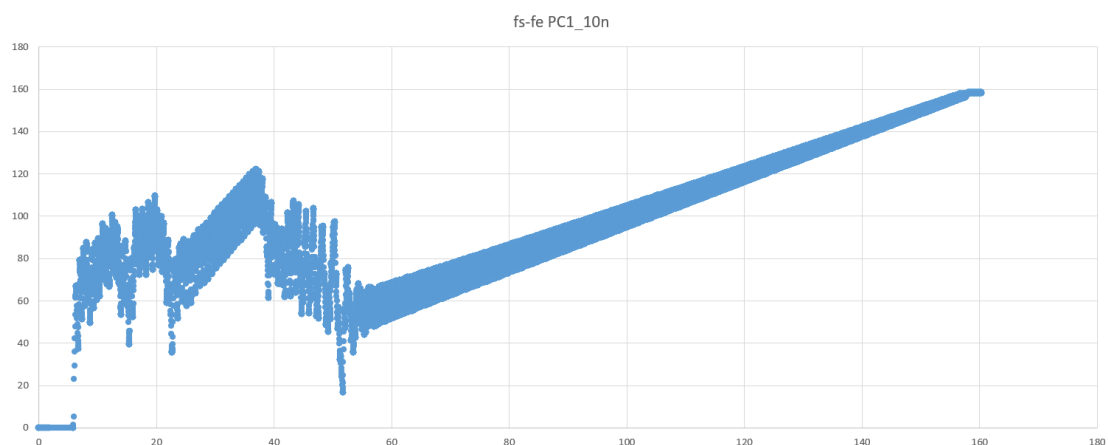
5. D'après partie 1, on peut trouver la relation entre $V1$ et f_{vco}

$$f_{vco} = \begin{cases} 1.954V1 & (V1 \leq 1) \\ 19.467V1 - 17.43 & (1 \leq V1 \leq 9) \\ 2.645V1 + 133.9 & (9 \leq V1 \leq 10) \end{cases}$$

fvco-V1

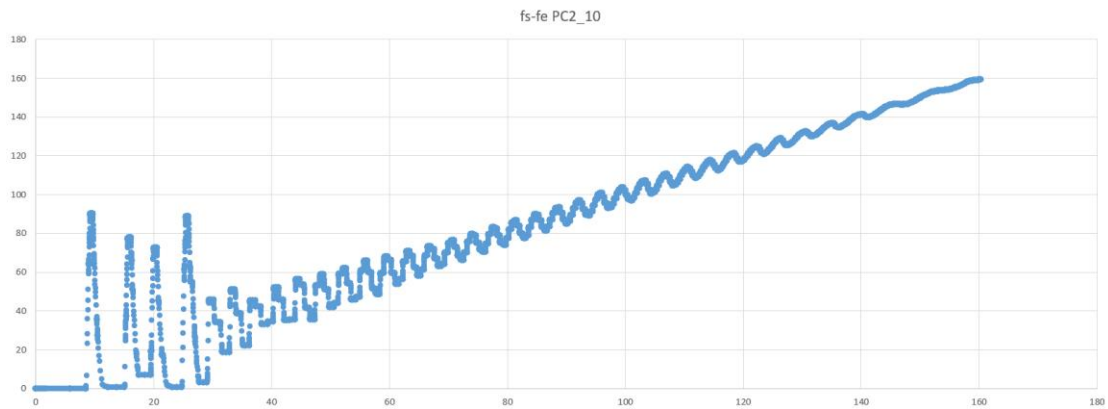


Alors on peut calculer f_s et f_e , ensuite trouver la relation entre eux :
Croissant PC1, $C_2 = 10nF$



$f_1 = 5.83kHz, f_2 = 159.89kHz$
plage de capture : $[5.83kHz, 159.89kHz]$

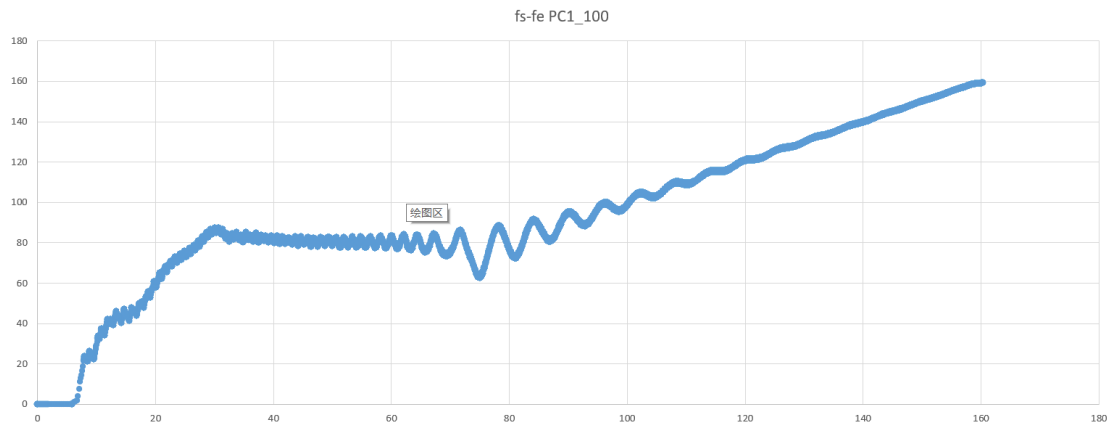
Croissant PC2, $C_2 = 10nF$



$$f_1 = 8.52kHz, f_2 = 160.34kHz$$

plage de capture : [8.52kHz, 160.34kHz]

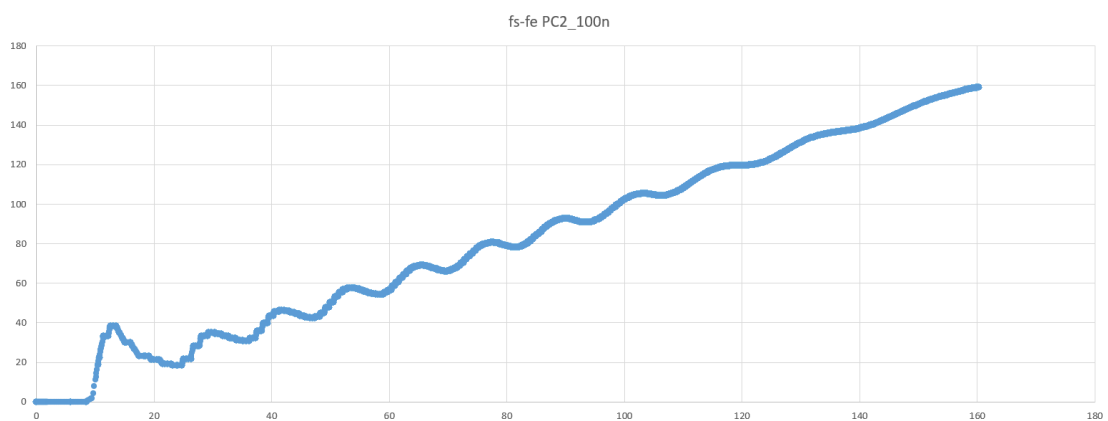
Croissant PC1, $C_2 = 100nF$



$$f_1 = 6.13kHz, f_2 = 160.34kHz$$

plage de capture : [6.13kHz, 160.34kHz]

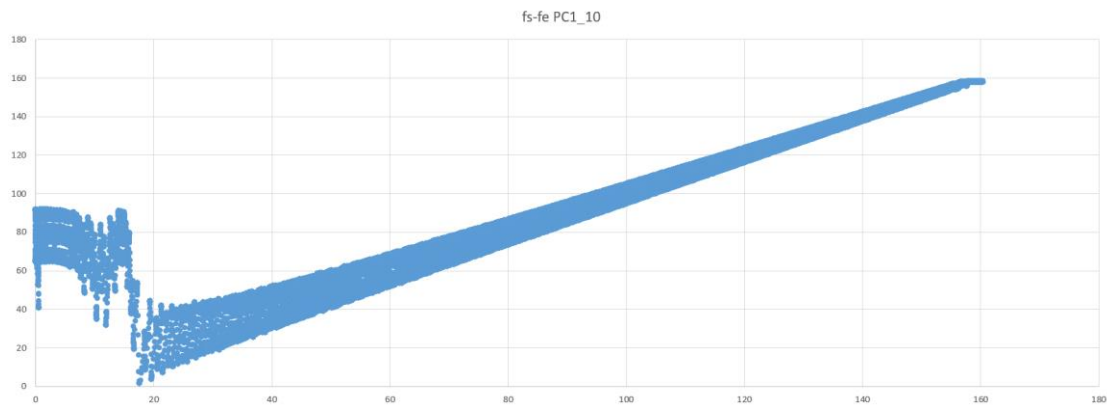
Croissant PC2, $C_2 = 100nF$



$$f_1 = 8.57kHz, f_2 = 160.34kHz$$

plage de capture : [8.57kHz, 160.34kHz]

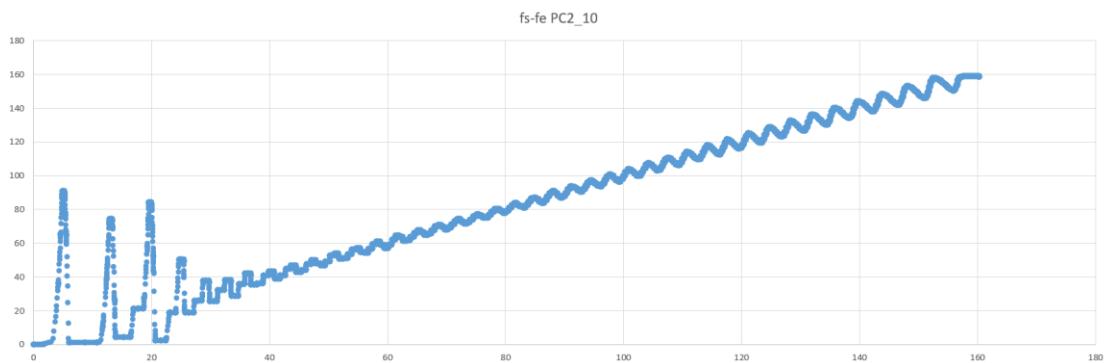
Décroissant PC1, $C_2 = 10nF$



$$f_1 = 0kHz, f_2 = 156.90kHz$$

plage de verrouillage : [0kHz, 156.90kHz]

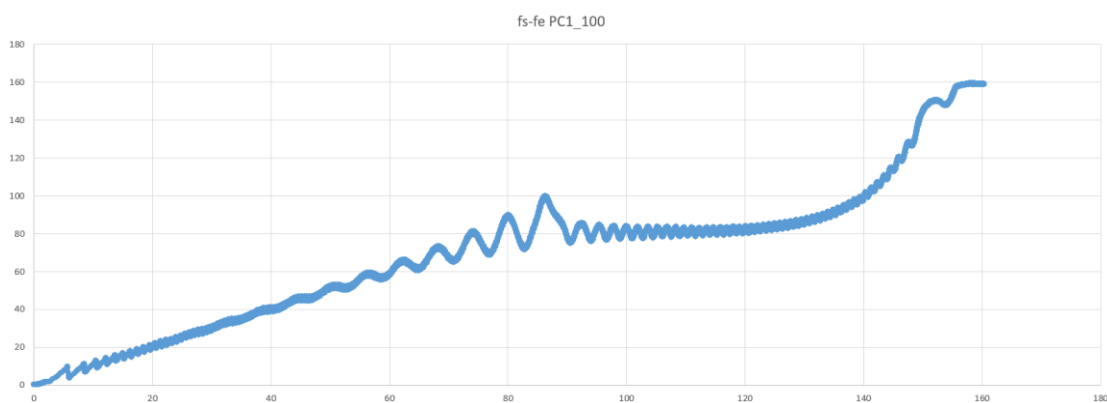
Décroissant PC2, $C_2 = 10nF$



$$f_1 = 0kHz, f_2 = 156.87kHz$$

plage de verrouillage : [0kHz, 156.87kHz]

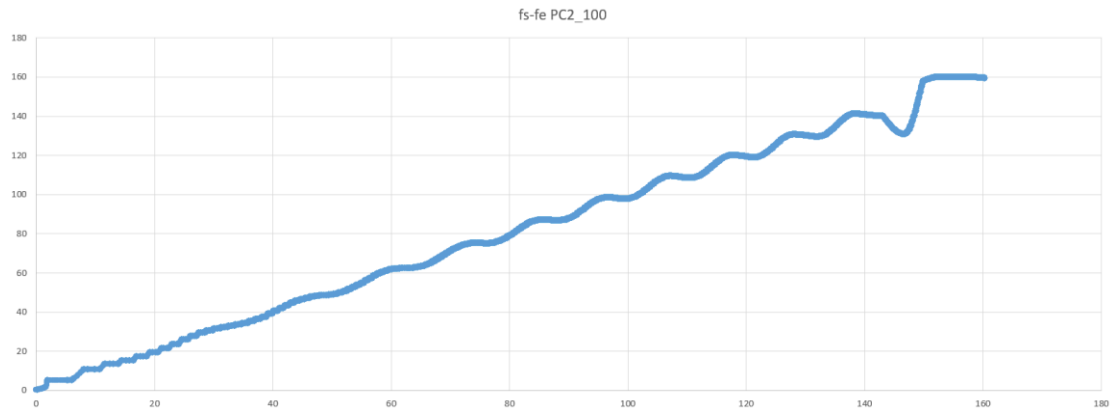
Décroissant PC1, $C_2 = 100nF$



$$f_1 = 0kHz, f_2 = 157.12kHz$$

plage de verrouillage : [0kHz, 157.12kHz]

Décroissant PC2, $C_2 = 100nF$

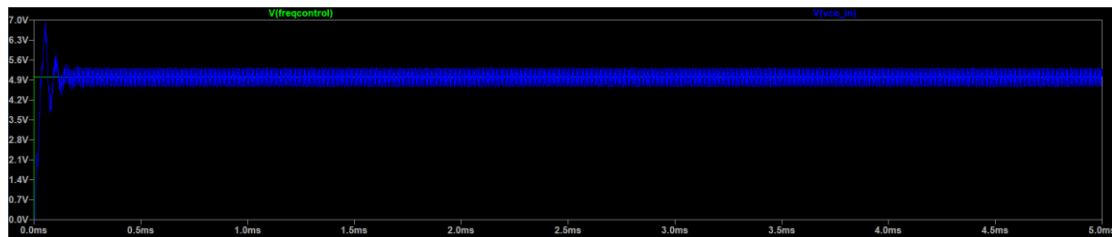


$$f_1 = 0kHz, f_2 = 151.05kHz$$

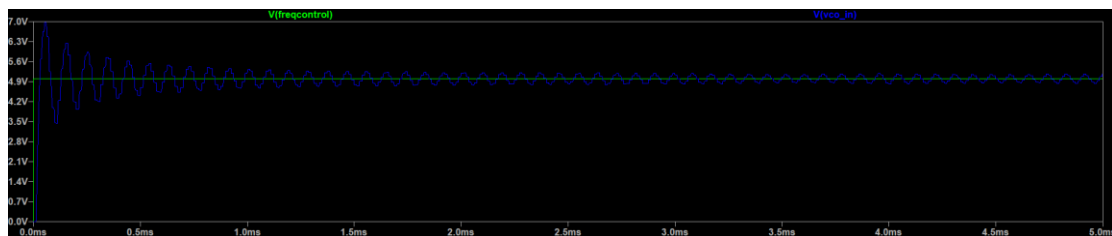
plage de verrouillage : [0kHz, 151.05kHz]

3. Réponse de la PLL à un échelon

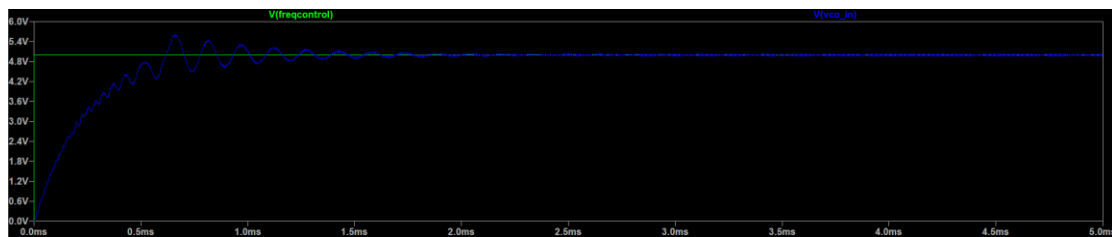
1. PC1, $C_2 = 10nF$



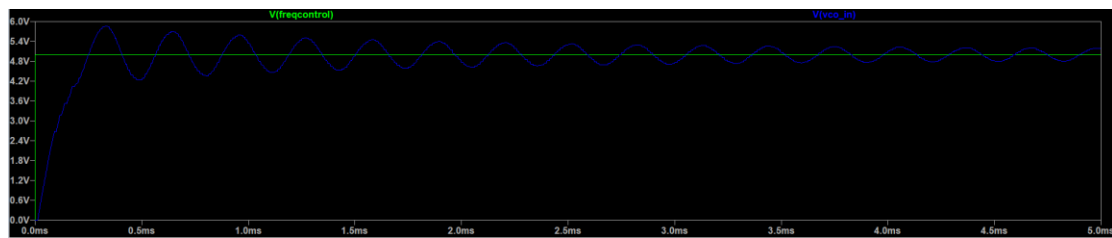
PC2, $C_2 = 10nF$



PC1, $C_2 = 100nF$



PC2, $C_2 = 100nF$



2. Le temps nécessaire pour atteindre 90% de la valeur de $V(f_{\text{control}})$

PC1, $C_2 = 10nF$

$$t_{90\%} = 131.768\mu s$$

PC2, $C_2 = 10nF$

$$t_{90\%} = 548.93\mu s$$

PC1, $C_2 = 100nF$

$$t_{90\%} = 0.75ms$$

PC2, $C_2 = 100nF$

$$t_{90\%} = 1.139ms$$

3. Temps caractéristiques des filtres utilisés.

PC1, $C_2 = 10nF$

$$t_{\text{carac}} = RC = 100\mu s$$

PC2, $C_2 = 10nF$

$$t_{\text{carac}} = RC = 100\mu s$$

PC1, $C_2 = 100nF$

$$t_{\text{carac}} = RC = 1ms$$

PC2, $C_2 = 100nF$

$$t_{\text{carac}} = RC = 1ms$$