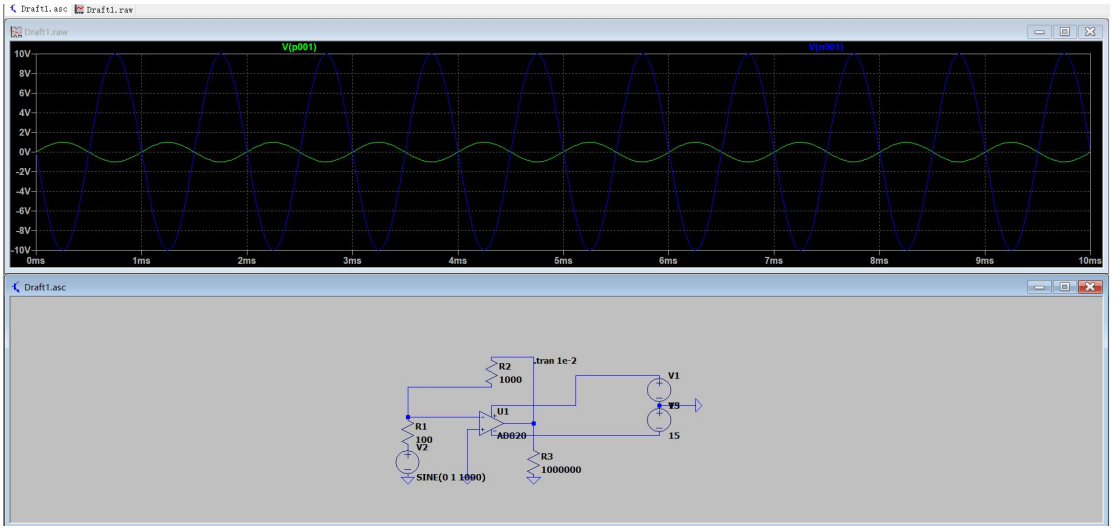
1. Étude statique

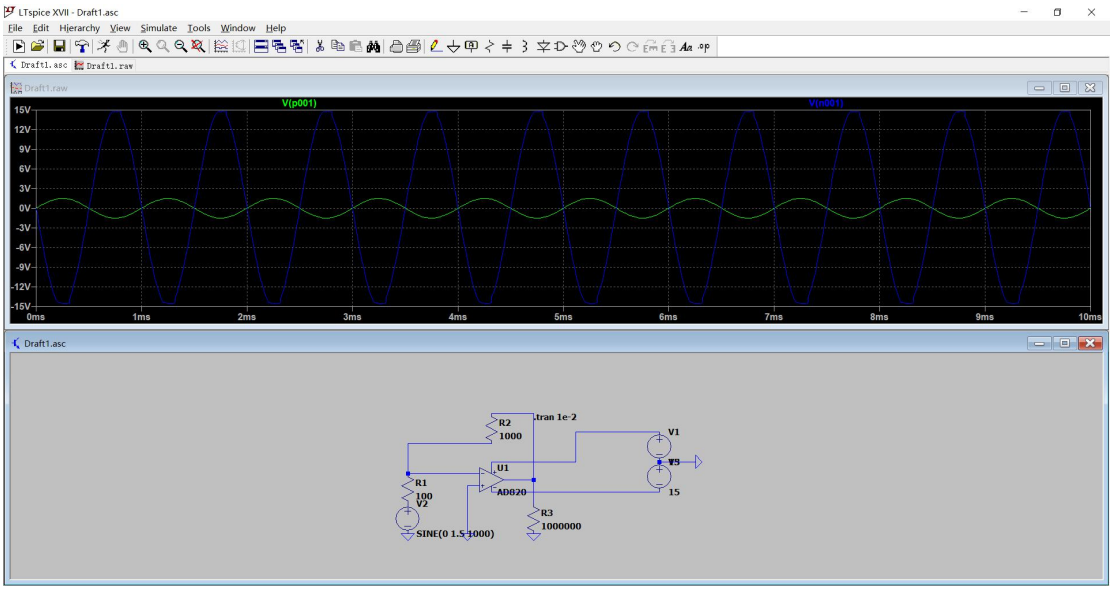
Q1



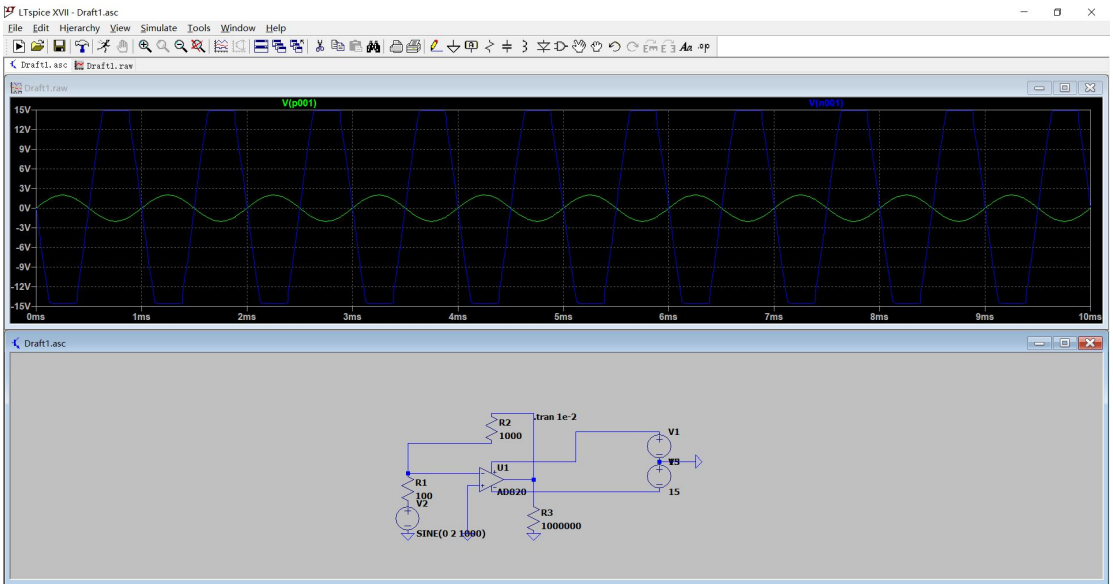
La figure en bleu est la sortie.

Q2

A=1.5V



A=2V

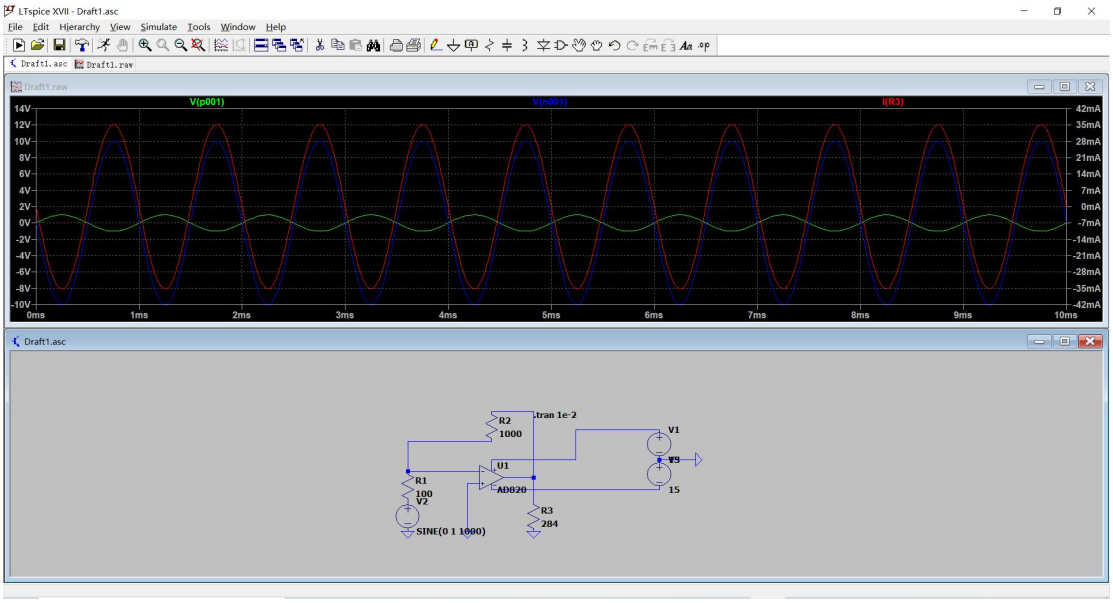


https://www.analog.com/media/en/technical-documentation/data-sheets/AD820.pdf

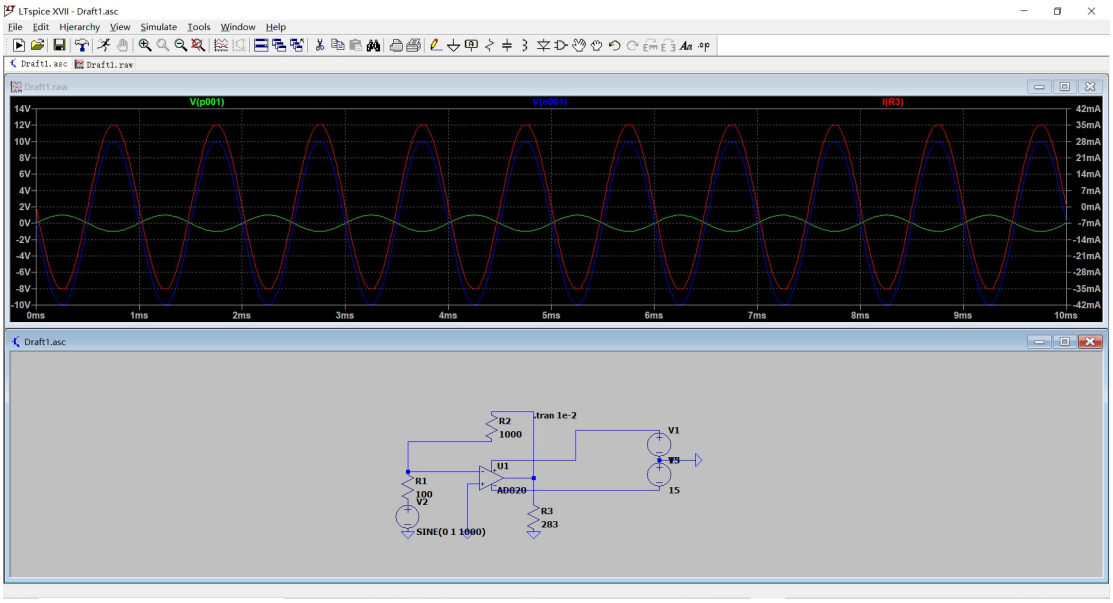
D’après le document, la valeur de saturation est cohérente, +/-15V pour AD820

Q3

R3=284Ω



R3=283Ω

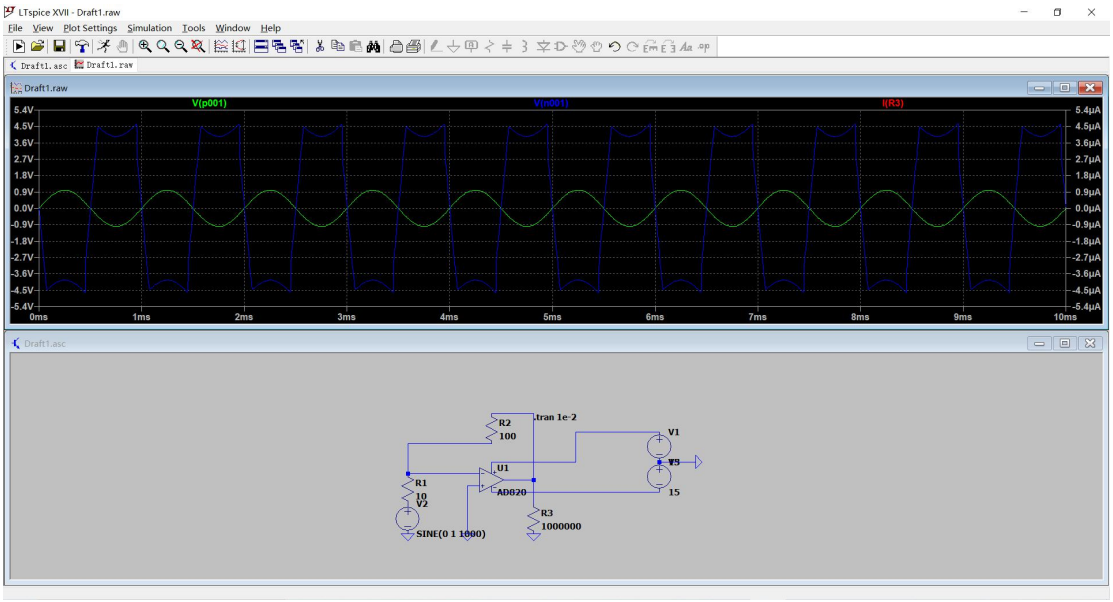


Donc, la valeur maximale est 35mA, c'est la courant saturée de AD820.

Q4

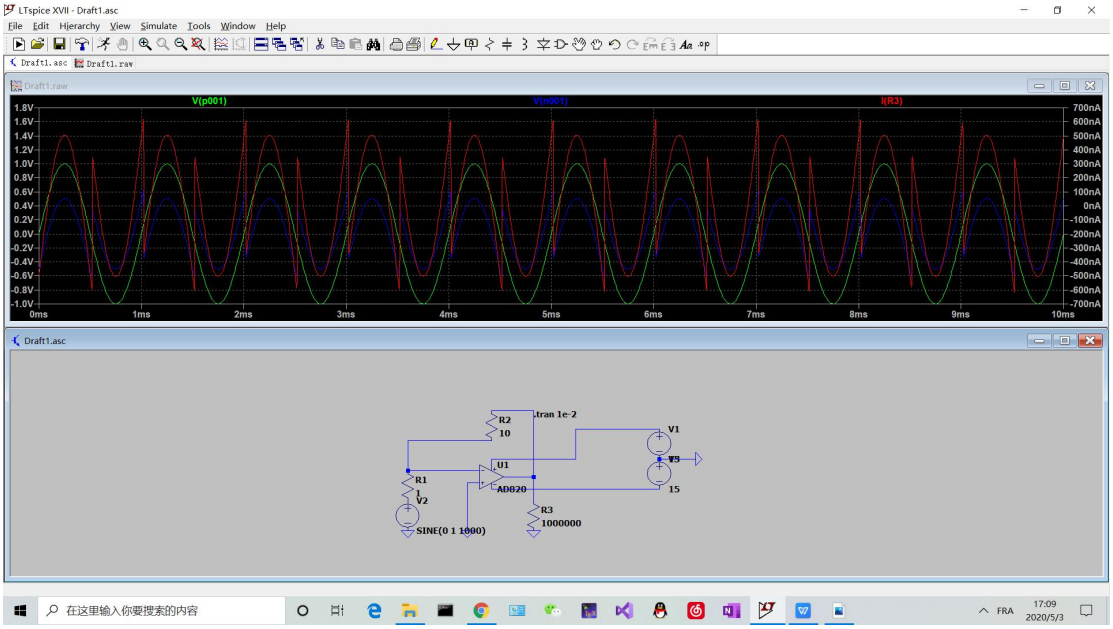
R1=10Ω

R2=100Ω

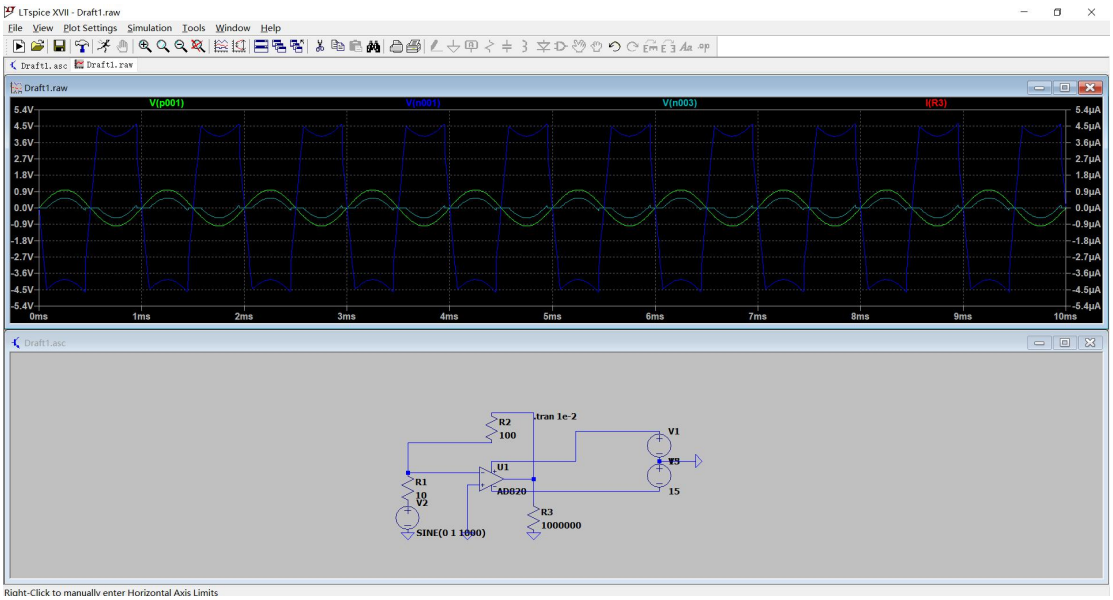


R1=1Ω

R2=10Ω

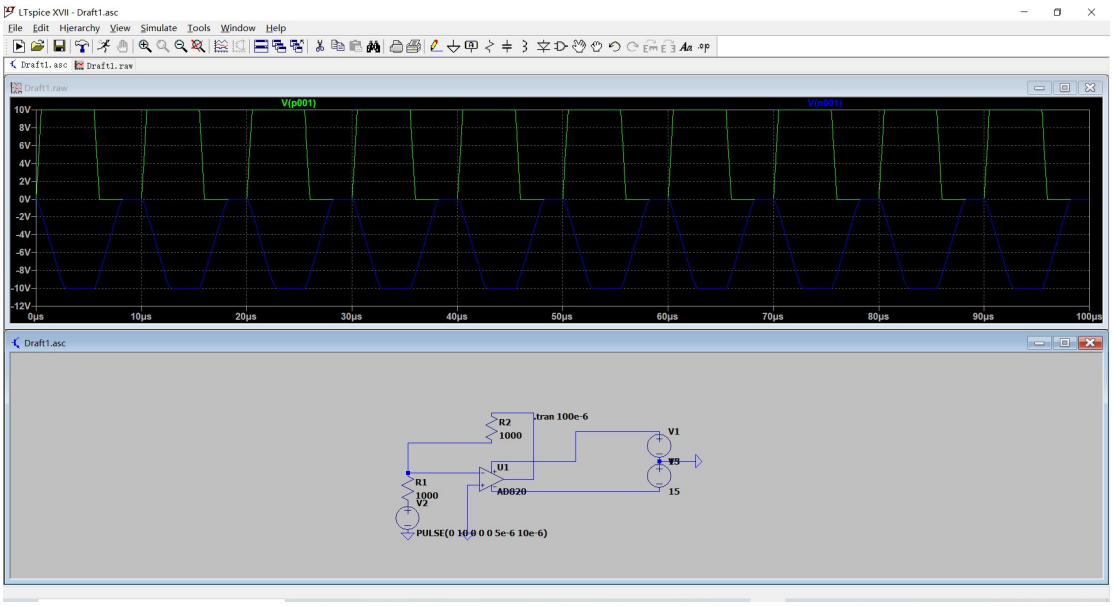


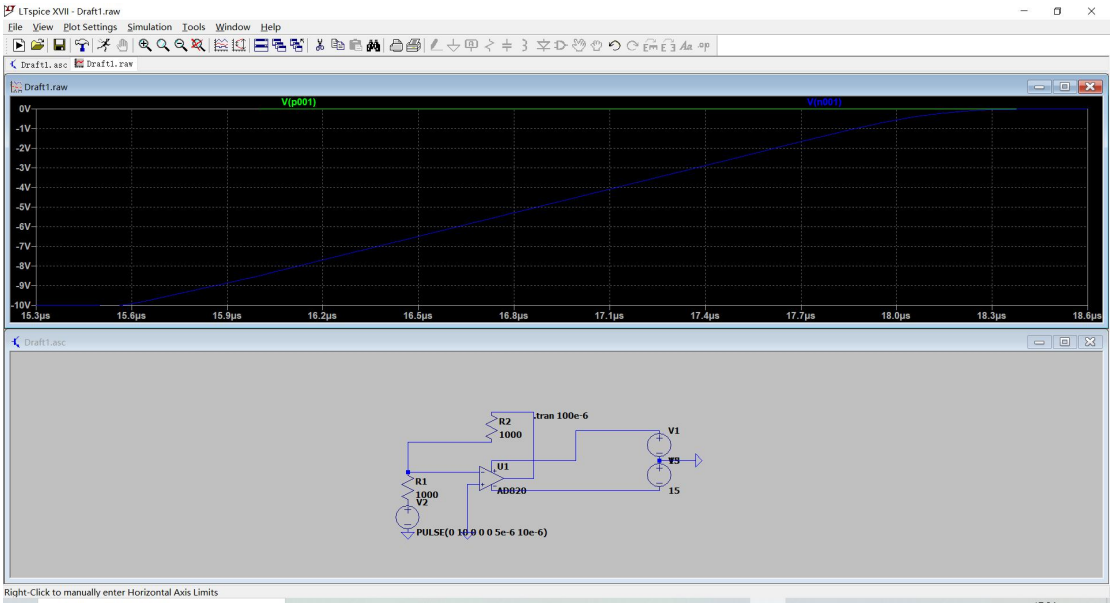
S’ils sont très petits, la valeur de V- ne peut pas rester équale à laqualle de V+, c’est-à-dire 0V, il ne peut pas rester dans la mode lineaire.



2. Étude dynamique

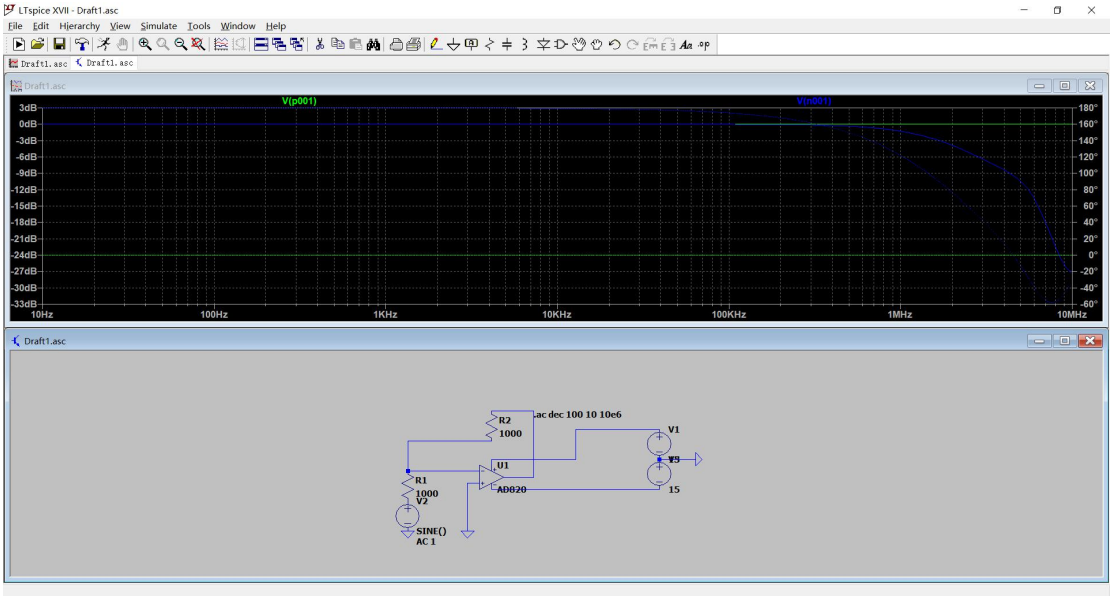
Q5

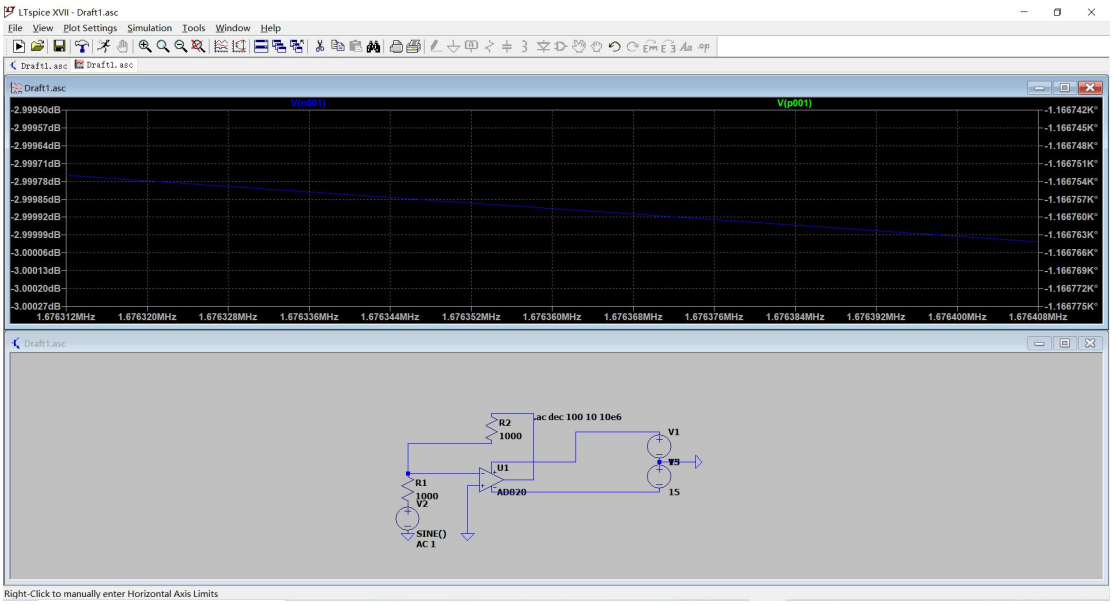




slew rate=10V/2.7µs=3.70V/µs≈3V/µs celle dans la fiche technique

Q6

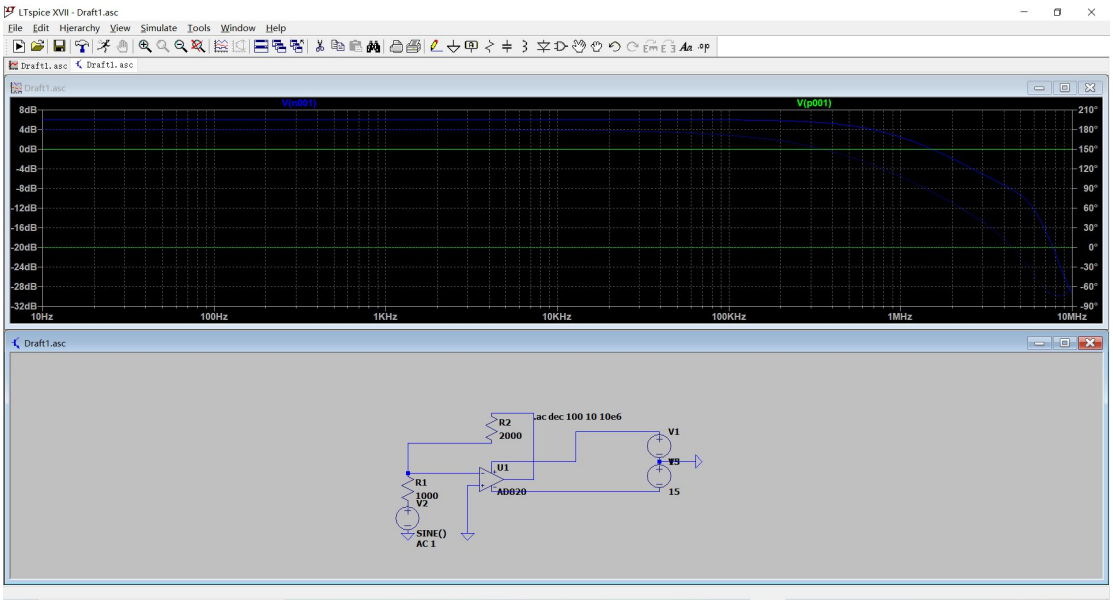


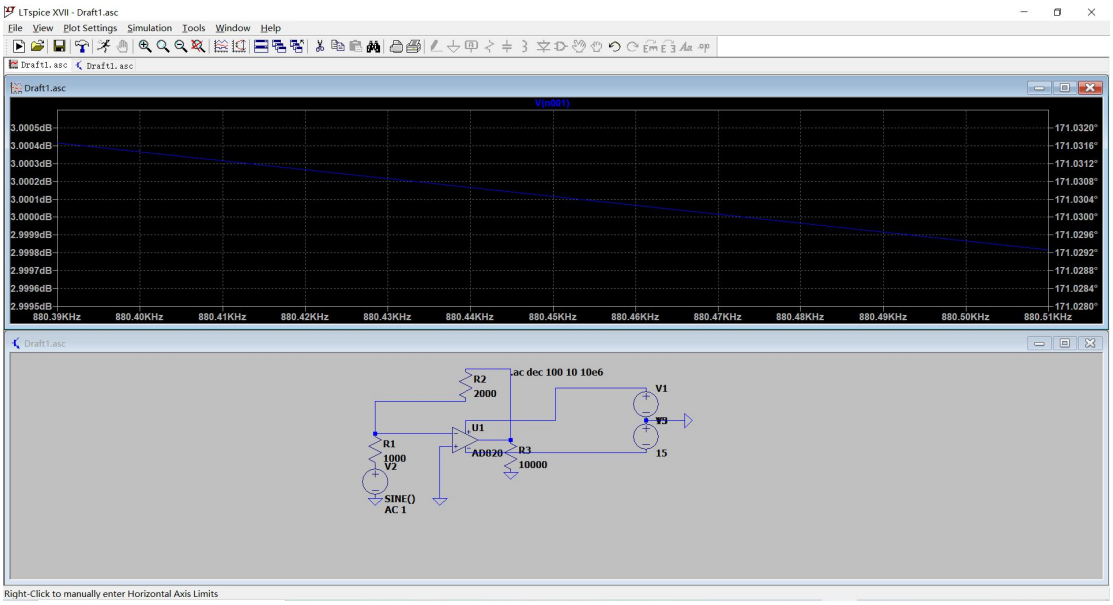


f=1.676397MHz

un peu plus petit que 1.8MHz, celle dans la fiche technique

Q7



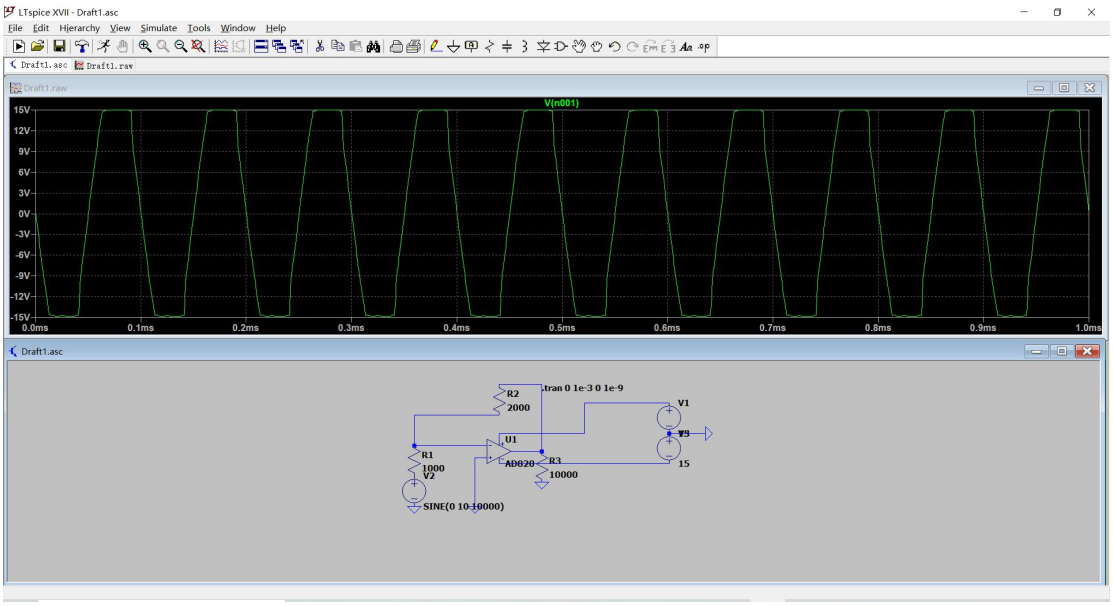


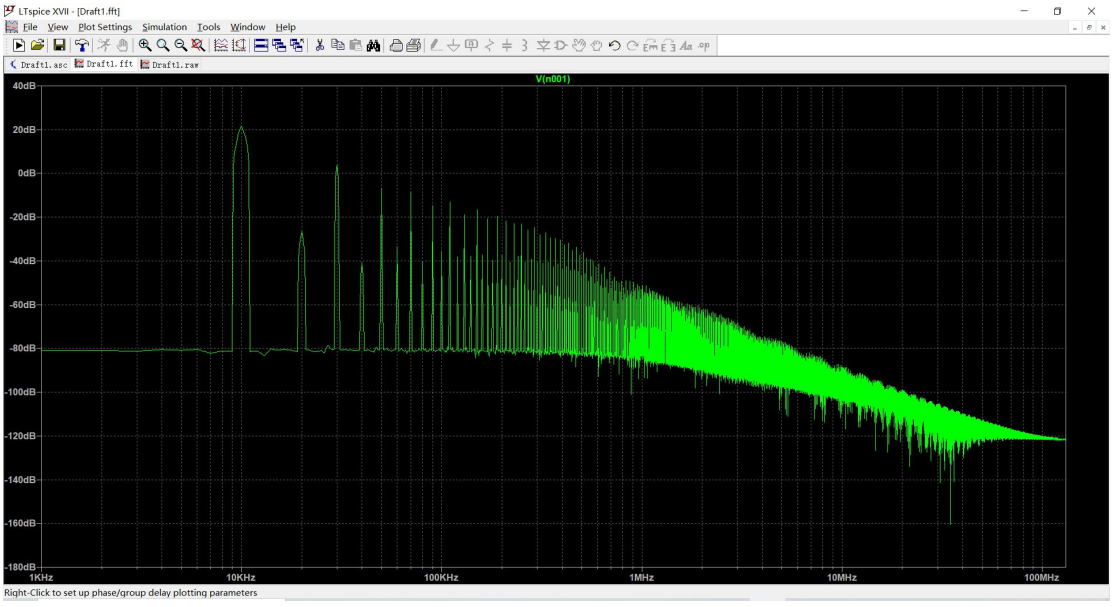
f=0.88047MHz

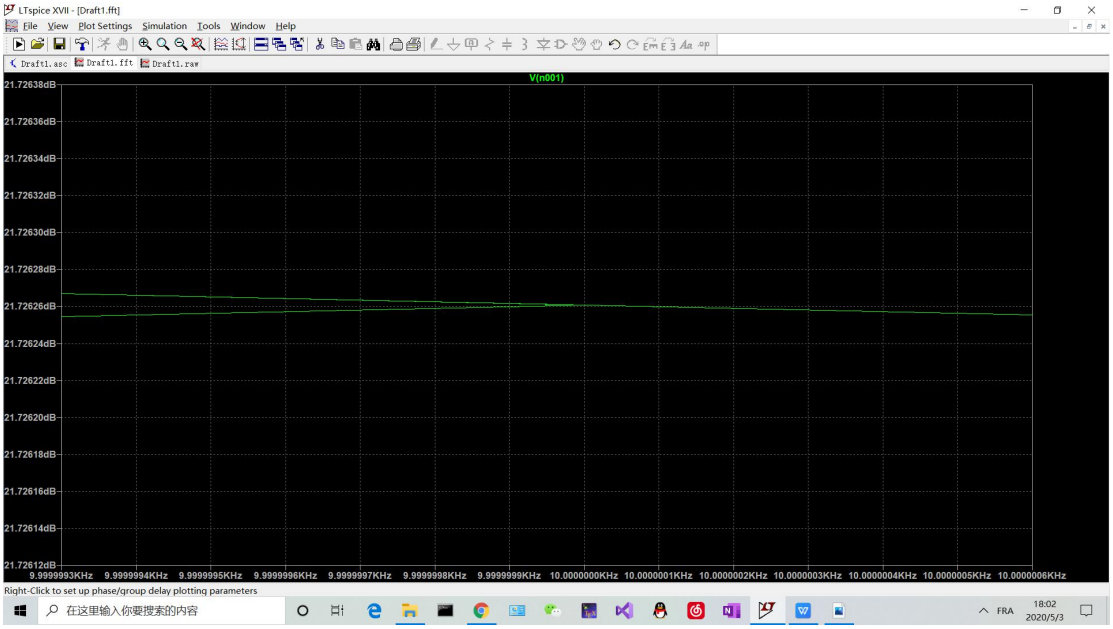
Donc, 2*0.88047≈1*1.67639

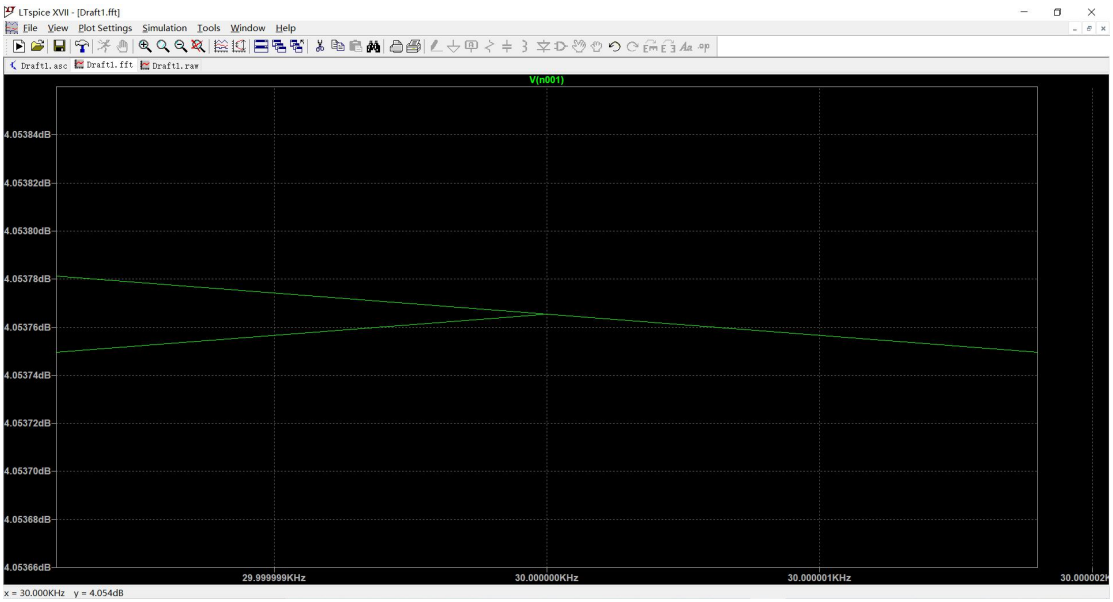
Le produit est constant.

Q8


LTspice XVII - Draft1.asc
File Edit Hierarchy View Simulate Tools Window Help
Draft1.asc Draft1.raw
Draft1.raw
V(n001)
15V
12V
9V
6V
3V
0V
-3V
-6V
-9V
-12V
-15V
0.0ms 0.1ms 0.2ms 0.3ms 0.4ms 0.5ms 0.6ms 0.7ms 0.8ms 0.9ms 1.0ms
Draft1.asc
R2
2000
.tran 0 1e-3 0 1e-9
V1
V3
15
U1
AD820
R3
10000
R1
1000
V2
SINE(0 10 10000)

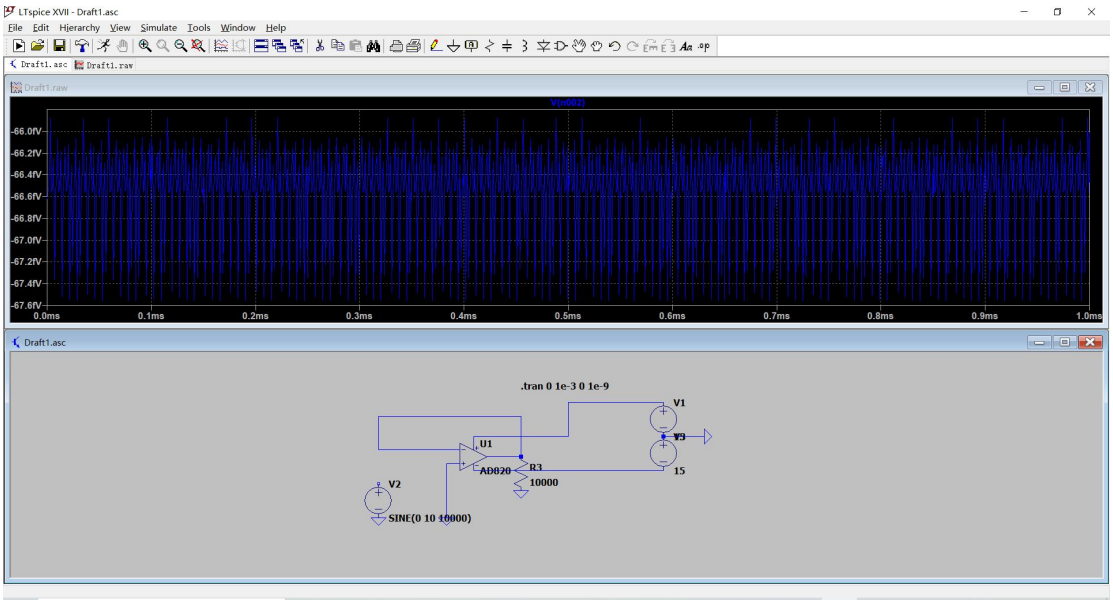

LTspice XVII - [Draft1.fft]
File View Plot Settings Simulation Tools Window Help
Draft1.asc Draft1.fft Draft1.raw
V(n001)
40dB
20dB
0dB
-20dB
-40dB
-60dB
-80dB
-100dB
-120dB
-140dB
-160dB
-180dB
1KHz 10KHz 100KHz 1MHz 10MHz 100MHz
Right-Click to set up phase/group delay plotting parameters

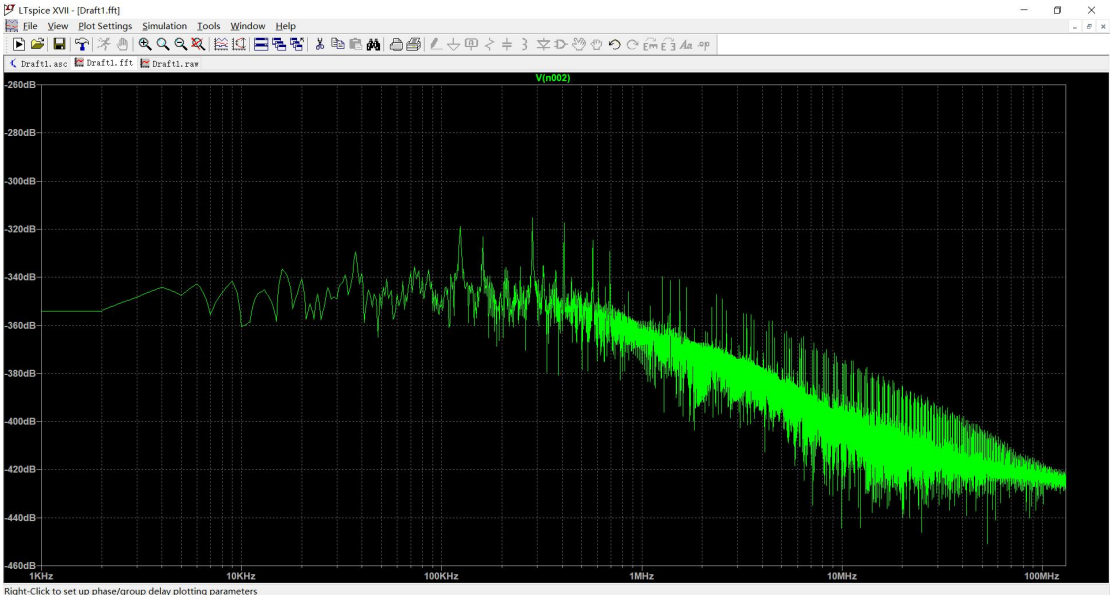


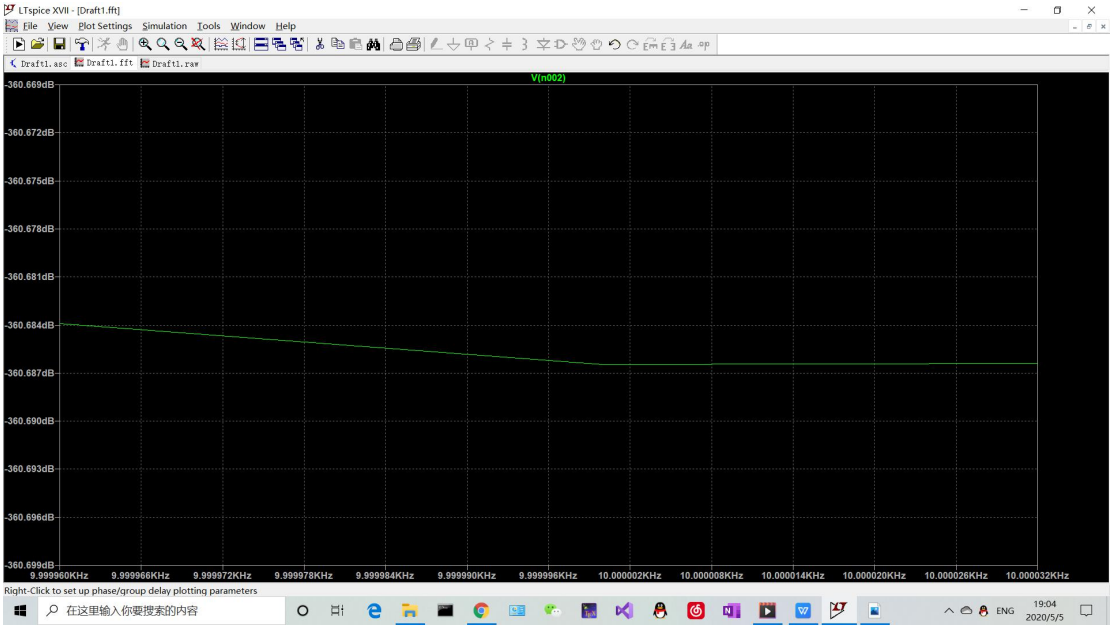


diff2=-21.72626-(-4.05377)=-17.67249dB

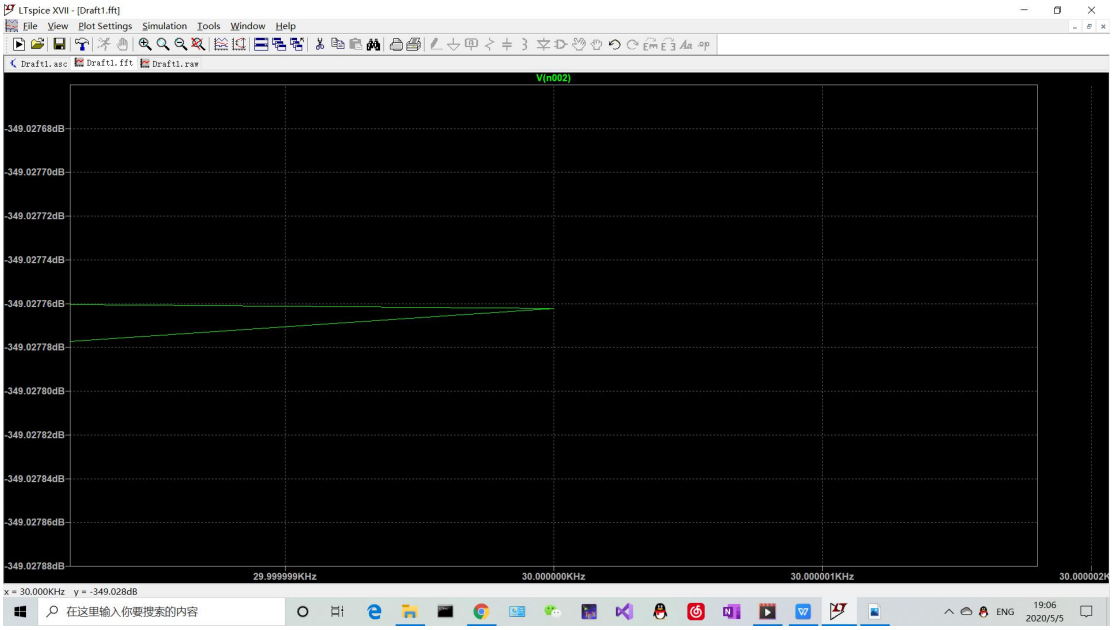
Les deux sont près de celles de fiche technique.


LTspice XVII - Draft1.asc
File Edit Hierarchy View Simulate Tools Window Help
Draft1.asc Draft1.raw
Draft1.raw
V(n002)
-66.0fV
-66.2fV
-66.4fV
-66.6fV
-66.8fV
-67.0fV
-67.2fV
-67.4fV
-67.6fV
0.0ms 0.1ms 0.2ms 0.3ms 0.4ms 0.5ms 0.6ms 0.7ms 0.8ms 0.9ms 1.0ms
Draft1.asc
.tran 0 1e-3 0 1e-9
V1
V3
15
U1
AD820
R3
10000
V2
SINE(0 10 10000)


LTspice XVII - [Draft1.fft]
File View Plot Settings Simulation Tools Window Help
Draft1.asc Draft1.fft Draft1.raw
V(n002)
-260dB
-280dB
-300dB
-320dB
-340dB
-360dB
-380dB
-400dB
-420dB
-440dB
-460dB
1KHz 10KHz 100KHz 1MHz 10MHz 100MHz
Right-Click to set up phase/group delay plotting parameters



-360.686dB



-349.028dB

la différence est 11.658dB