

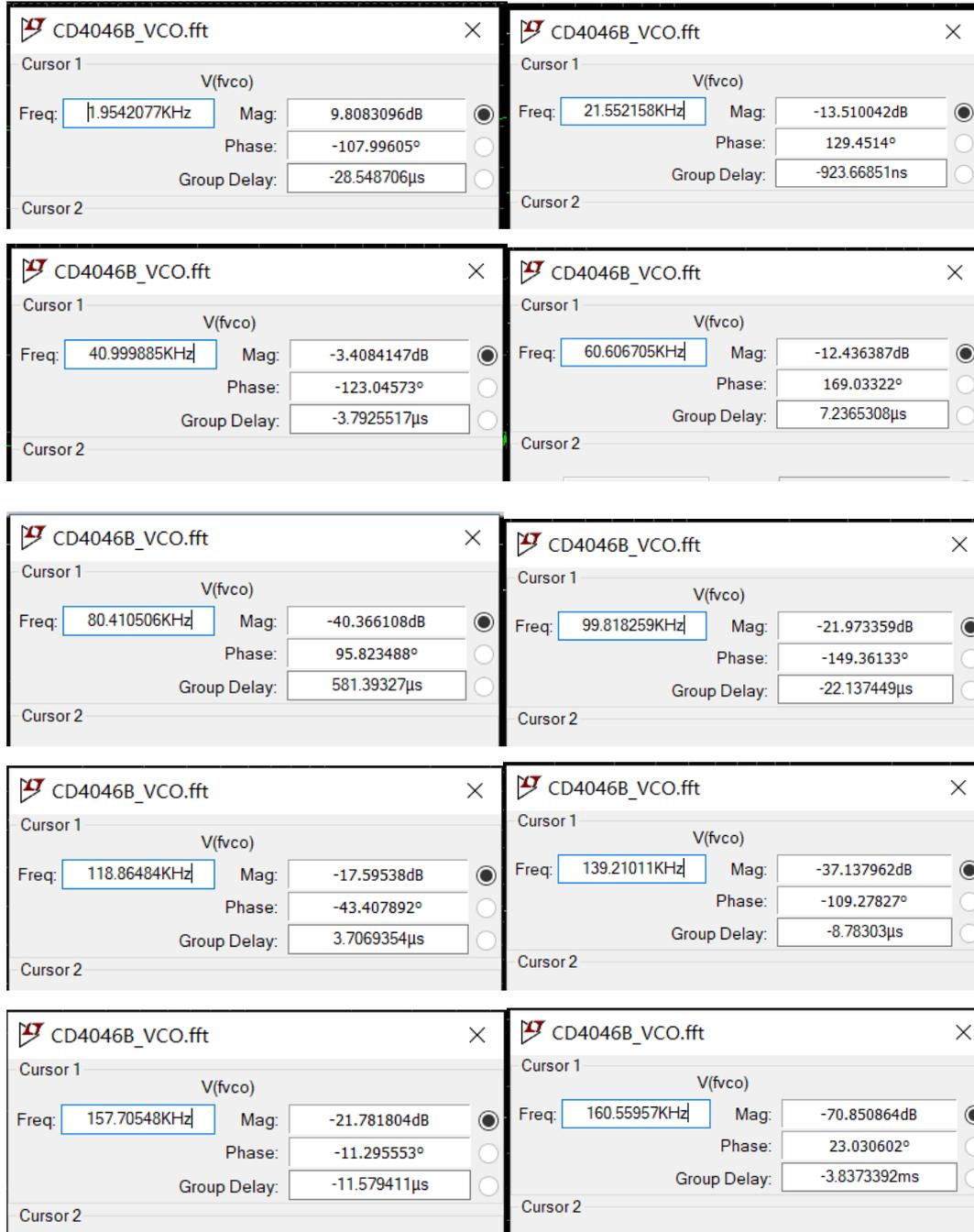
Devoir fréquence

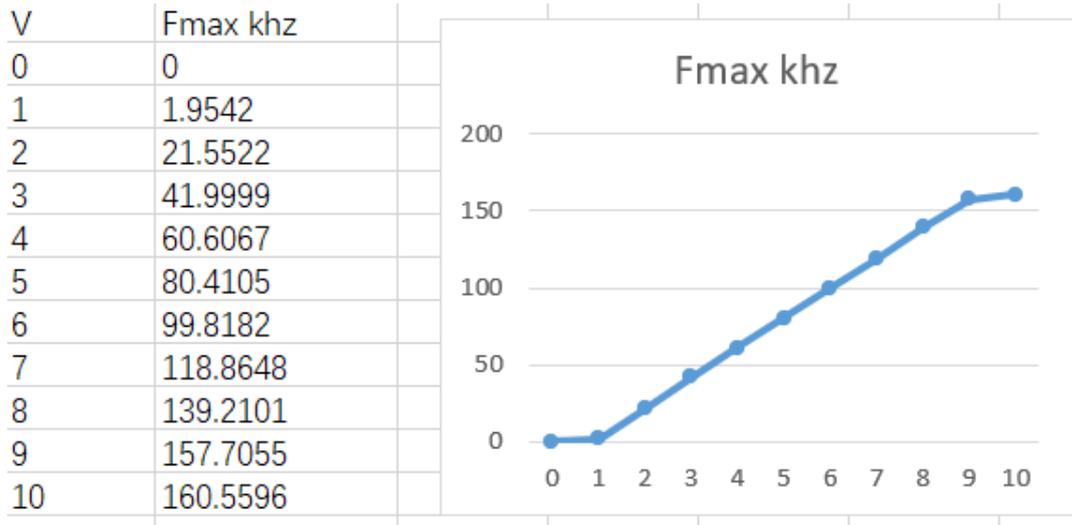
Odile XING Yimeng ZY1824128/14241044

I Caractérisation du VCO

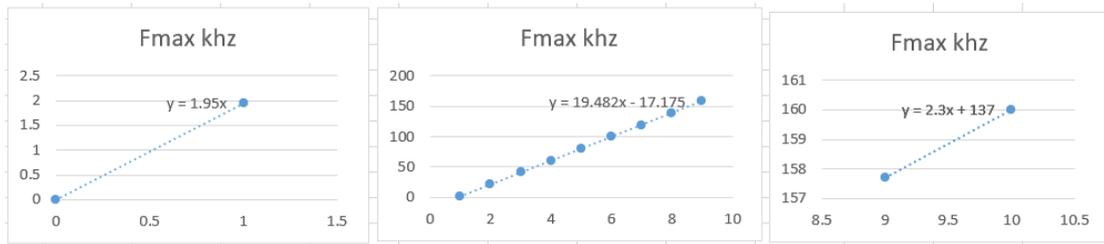
1. Avec la figure 7, $f_0 = 80\text{kHz}$, alors $f_{\text{max}} = 160\text{kHz}$

2. Les résultats suivants sont pour les V_1 de 1 à 10V.



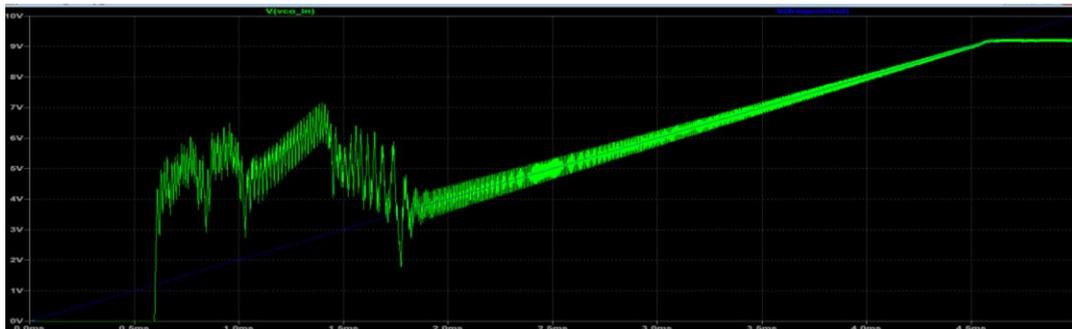


Ce VCO fonctionne bien en comparant avec la fiche technique, et les fonctions entre fs et V sont les suivantes :

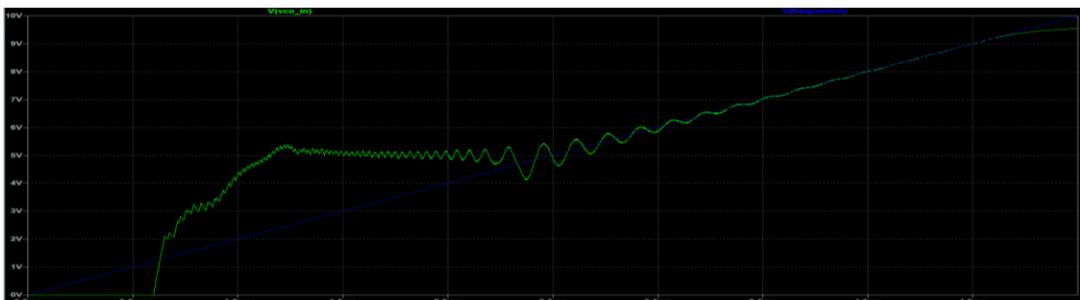


II Mesure des plages de capture et de verrouillage

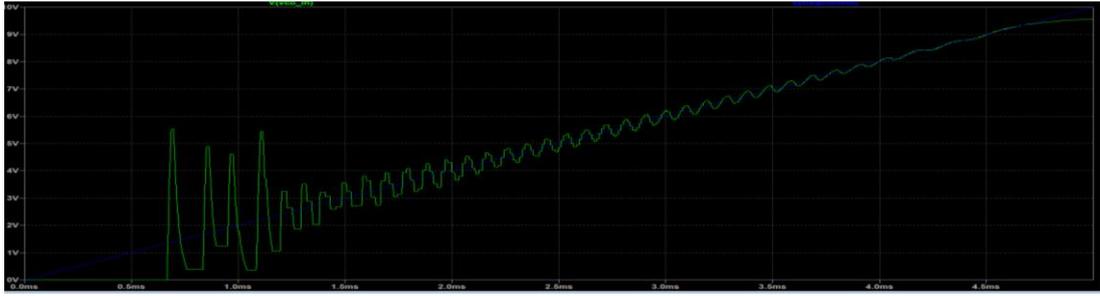
3.



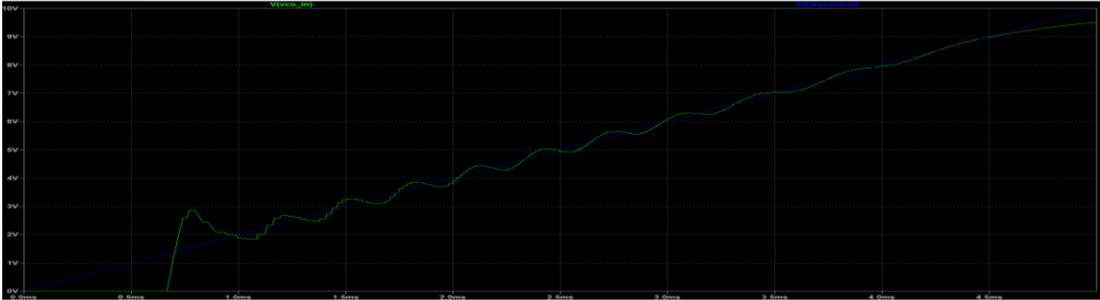
Cr_pc1_10n



Cr_pc1_100n

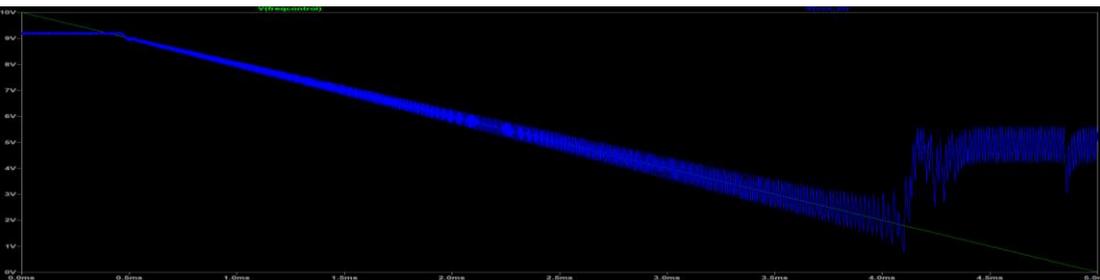


Cr_pc2_10n

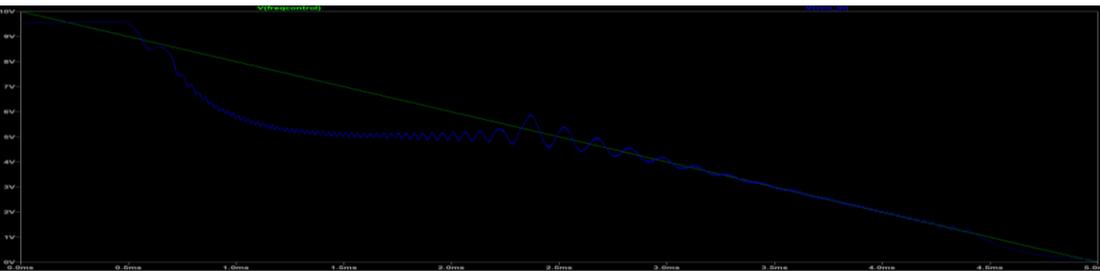


Cr_pc2_100n

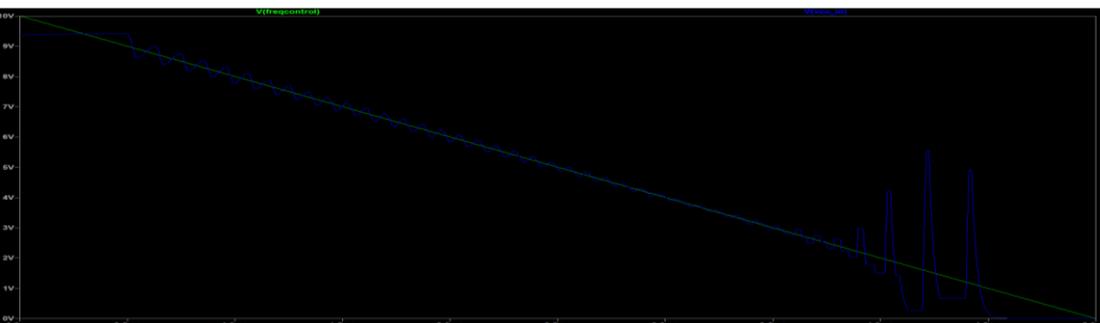
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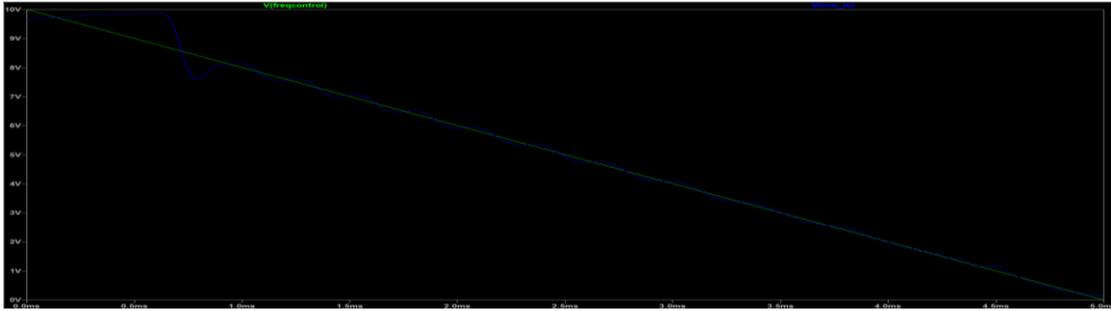
De_pc1_10n



De_pc1_100n

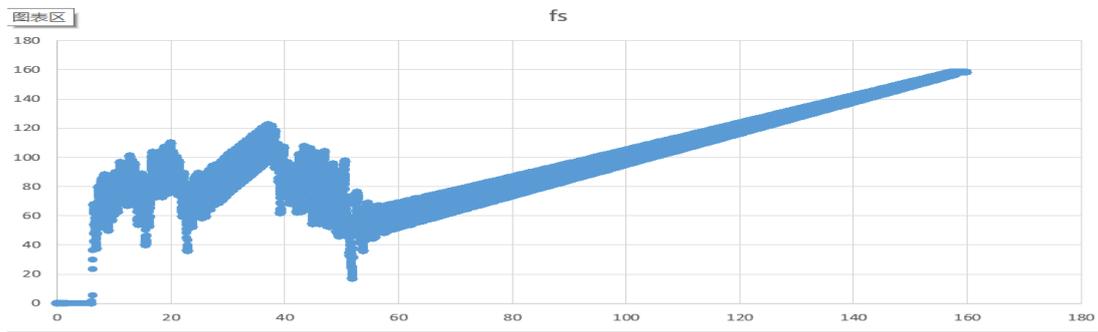


De_pc2_10n



De_pc2_100n

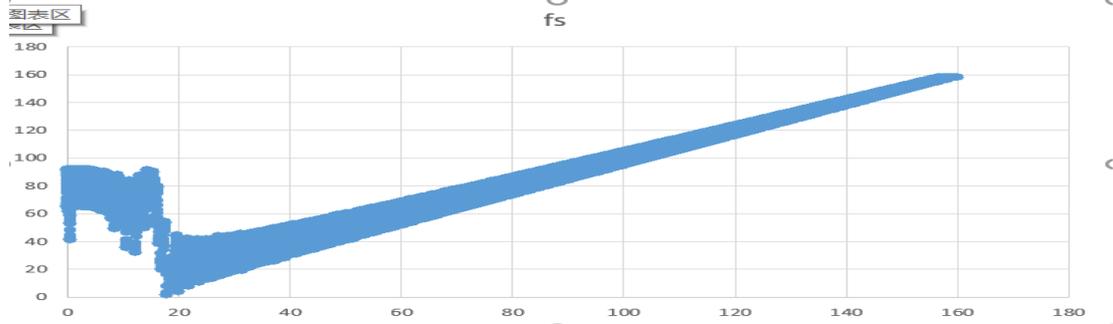
5.



Cr_pc1_10n

F1=6.1kHz

F2=159.98kHz



De_pc1_10n

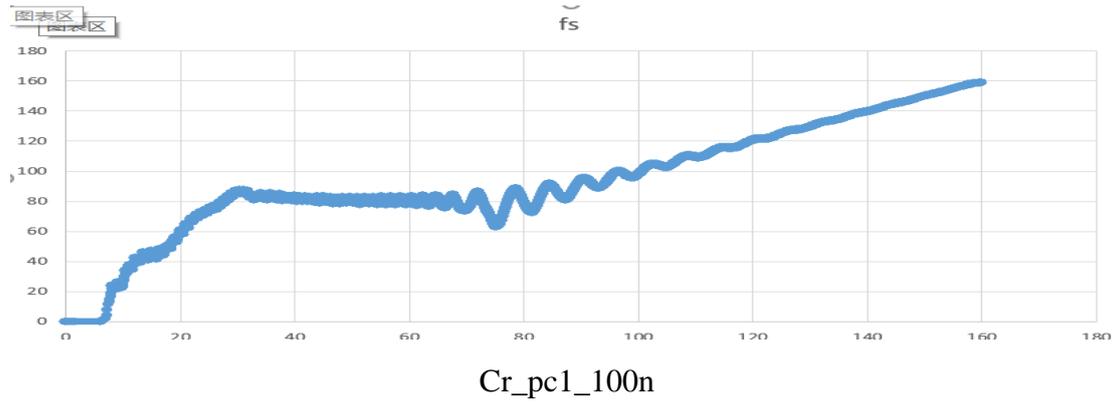
F1=0

F2=155.51kHz

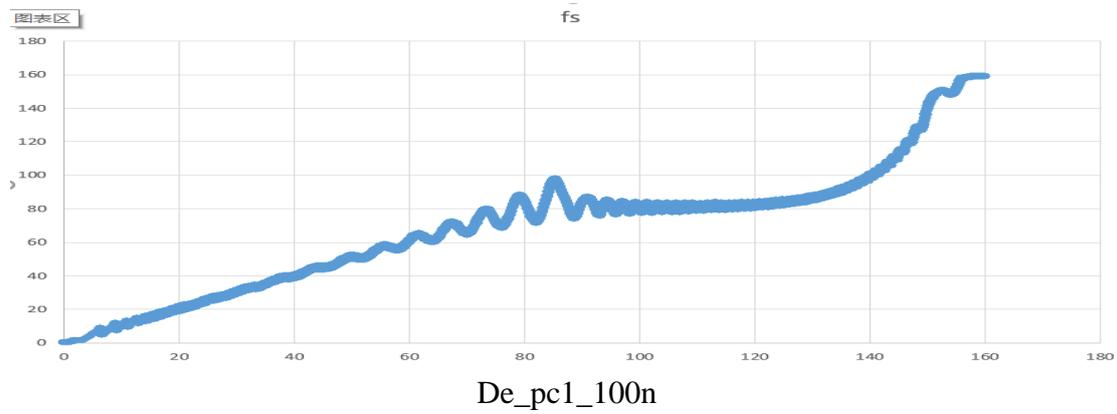
10nF_pc1 :

Plage de capture : 6.1-155.51kHz

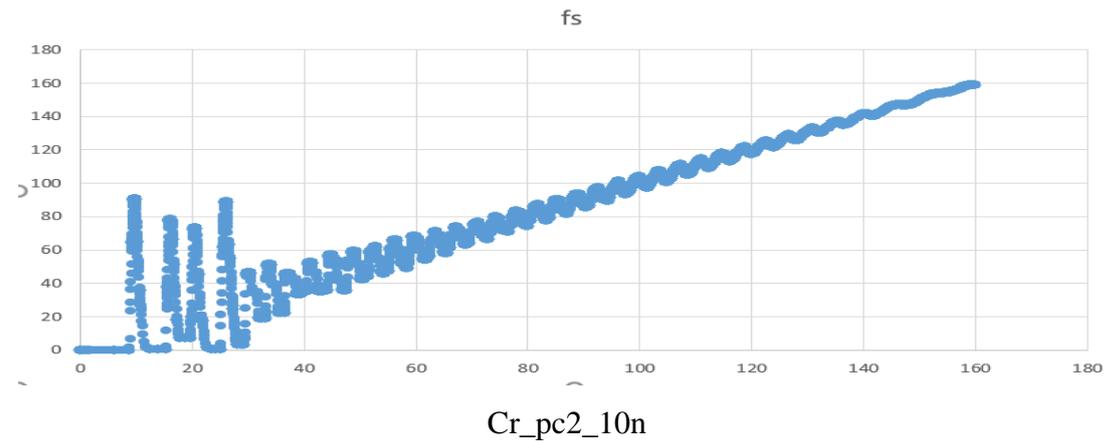
Plage de verrouillage : 0-159.98kHz



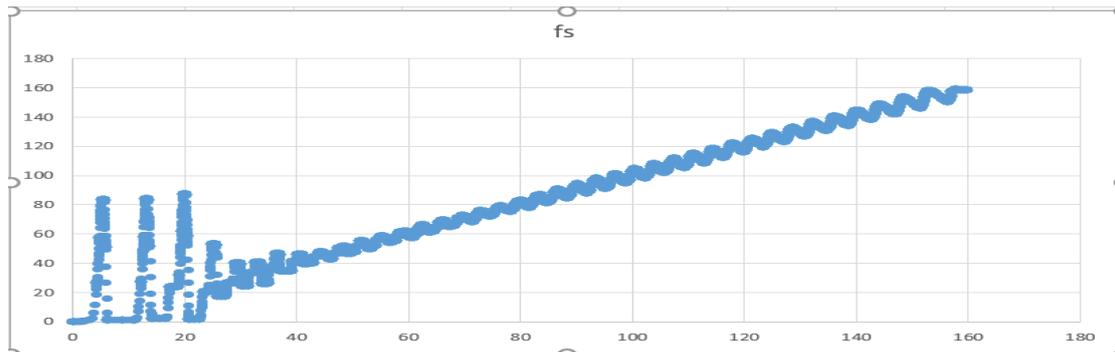
F1=6.59kHz
 F2=160kHz



F1=0
 F2=155.86kHz
 100nF_pc1 :
 Plage de capture : 6.59-155.86kHz
 Plage de verrouillage : 0-160kHz



F1=8.79kHz
 F2=160kHz



De_pc2_10n

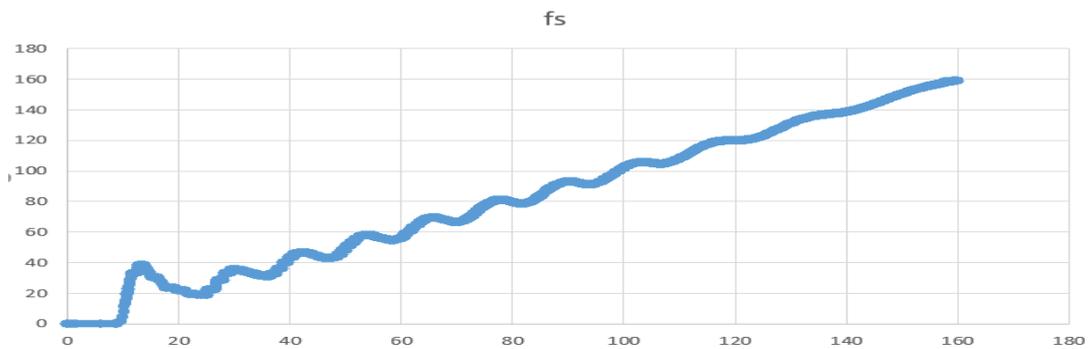
F1=3.25kHz

F2=157.01kHz

10nF_pc2 :

Plage de capture : 8.79-157.01kHz

Plage de verrouillage : 3.25-160kHz

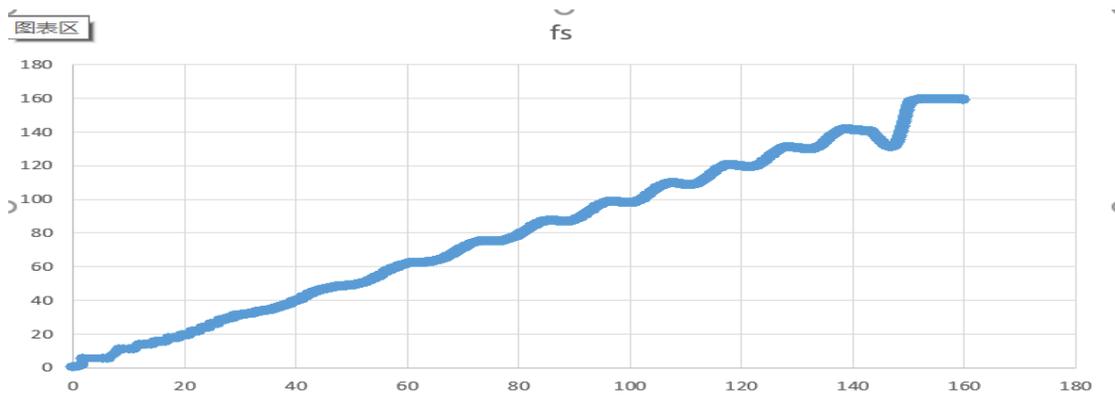


Cr_pc2_100n

F1=9.07kHz

F2=160kHz

图表区



De_pc2_100n

F1=0

F2=150.13kHz

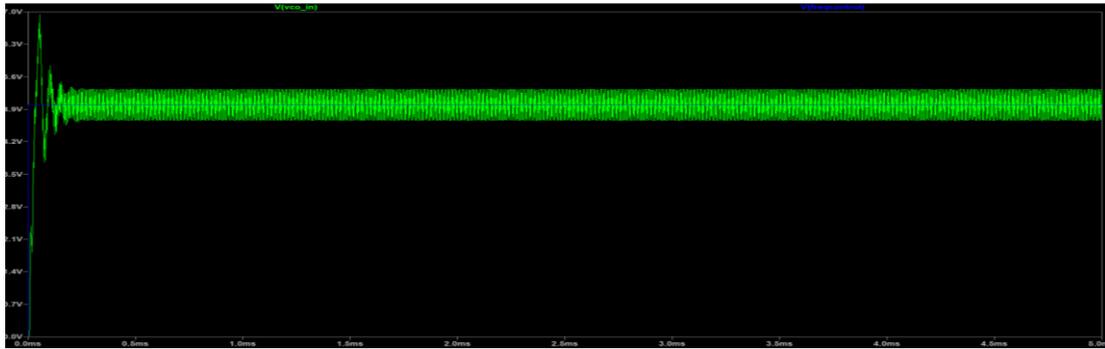
100nF_pc2 :

Plage de capture : 9.07-150.13kHz

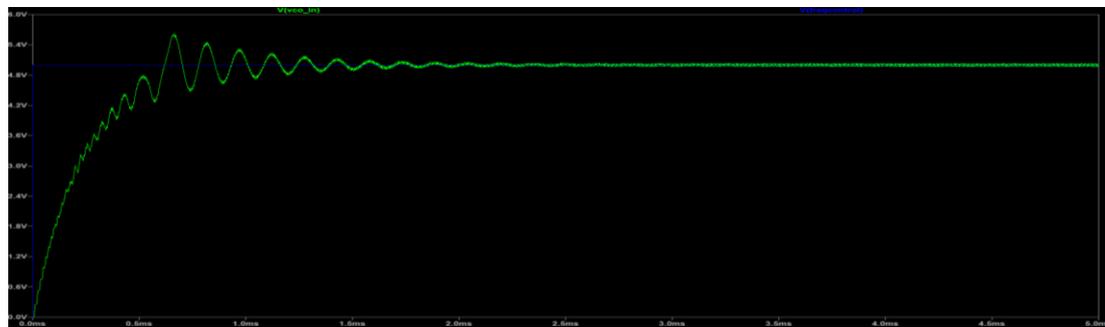
Plage de verrouillage : 0-160kHz

III Réponse de la PLL à un échelon

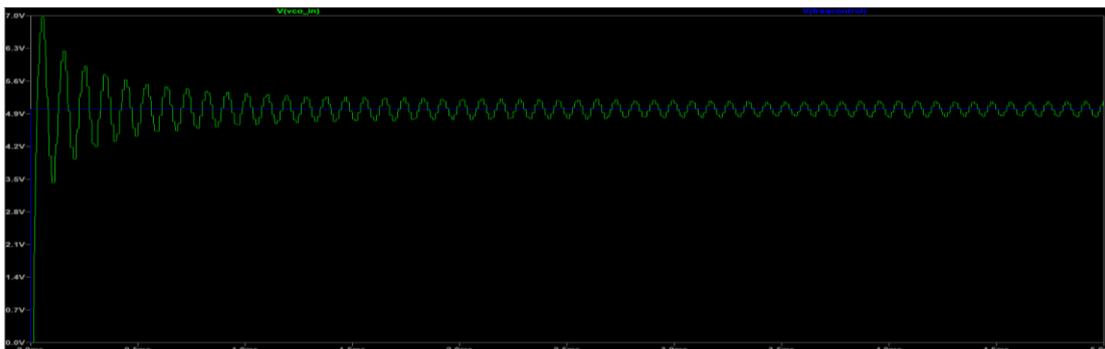
1.



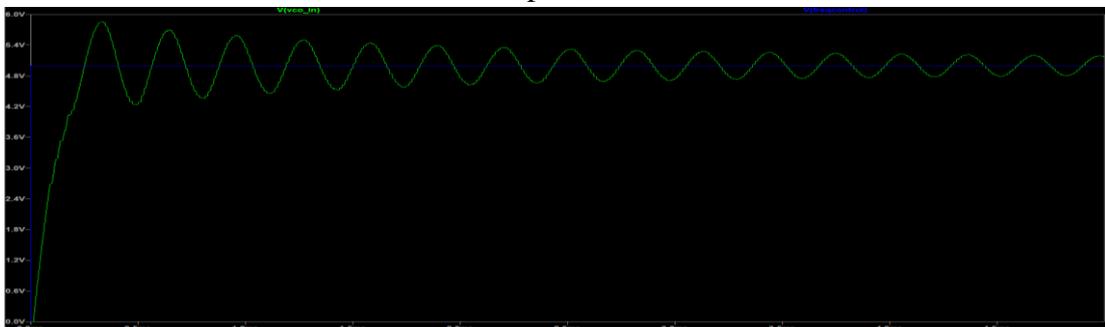
Ec_pc1_10n



Ec_pc1_100n

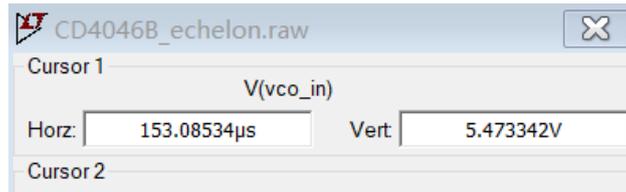


Ec_pc2_10n

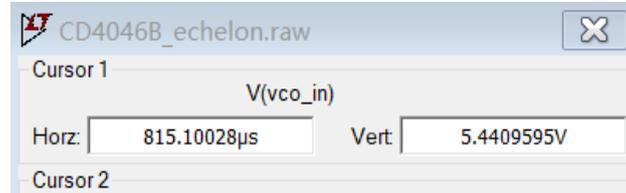


Ec_pc2_100n

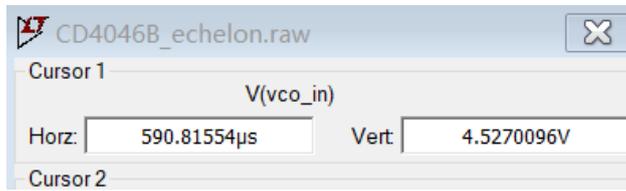
2.



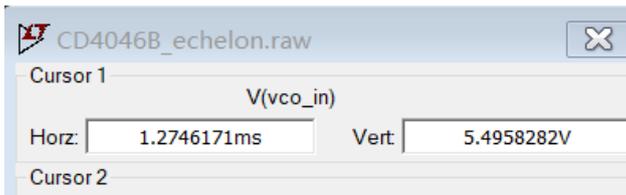
Ec_pc1_10n



Ec_pc1_100n



Ec_pc2_10n



Ec_pc2_100n

3. $\tau = RC$, $R_3 = 1.8k\Omega$, alors $\tau_{C2=10nF} = 18\mu s$, $\tau_{C2=100nF} = 180\mu s$, les résultats mesurés sont supérieurs aux résultats calculés.